



正基科技股份有限公司

SPECIFICATION

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PRODUCT NAME : AP6255

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Company	
Representative Signature	

PREPARED	REVIEW		APPROVED	DCC ISSUE
	PM	QA		

AMPAK

AP6255

WiFi 11ac + Bluetooth V4.2
Module Spec Sheet

Revision History

Date	Revision Content	Revised By	Version
2015/04/09	- Preliminary	Gary	1.0
2015/04/26	- Add GPIO pin definition	Gary	1.1
2016/06/20	- Modify BT Specification	Richard	1.2
2016/08/30	- Modify Dimensions	Richard	1.3
2017/02/06	- Modify BT output power spec	Richard	1.4

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1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the Wi-Fi, Bluetooth functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11a/b/g/n/ac Access Points in the wireless LAN.

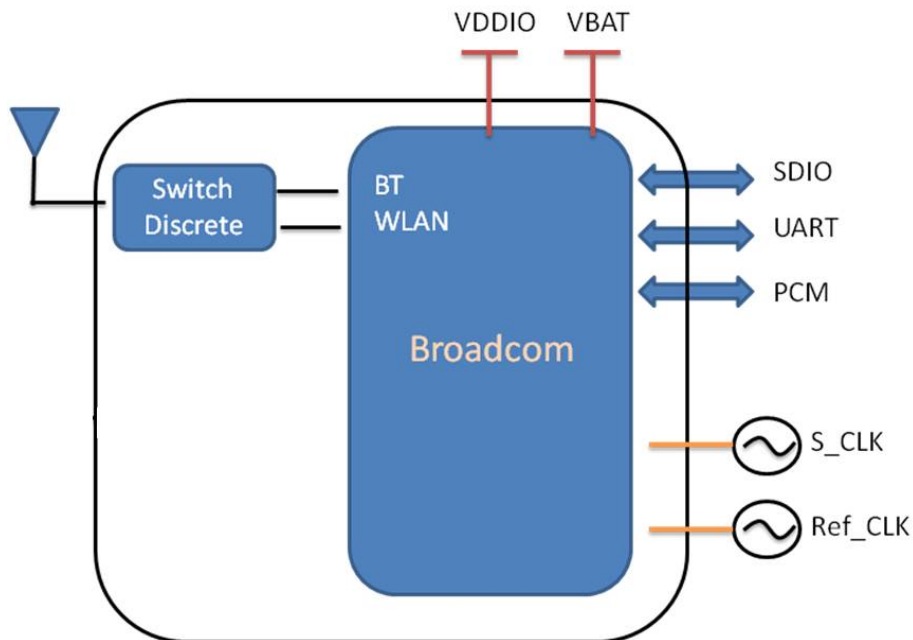
The wireless module complies with IEEE 802.11 a/b/g/n/ac standard and it can achieve up to a speed of 433.3Mbps with single stream in 802.11ac draft to connect to the wireless LAN. The integrated module provides SDIO interface for Wi-Fi, UART / PCM interface for Bluetooth.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

2. Features

- IEEE 802.11a/b/g/n/ac dual-band radio with virtual-simultaneous dual-band operation
- Single-stream spatial multiplexing up to 433.3 Mbps data rate.
- Supports 20, 40, 80 MHz channels with optional SGI(256 QAM modulation)
- Supports Bluetooth V4.2+EDR with integrated PA for Class 1.5 and Low Energy (BLE).
- Concurrent Bluetooth, and WLAN operation
- Simultaneous BT/WLAN receive with single antenna
- Supports standard SDIO v3.0 and backward compatible with SDIO v2.0 host interfaces.
 - SDIO v3.0(4-bit) — up to 208 MHz clock rate in SDR104 mode
- BT host digital interface:
 - UART (up to 4 Mbps)
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

A simplified block diagram of the module is depicted in the figure below.



3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

4. General Specification

4.1 General Specification

Model Name	AP6255
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 12 x 12 x 1.5 (typical) mm
WiFi Interface	SDIO v2.0/v3.0
BT Interface	UART / PCM
Operating temperature	-30°C to 65°C
Storage temperature	-40°C to 105°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Optimal RF performance specified in the data sheet, however, is guaranteed only for -20~55 °C

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	6	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.9	V

4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	65	deg.C
VBAT	3.13	3.6	4.8	V
VDDIO	1.71	1.8	3.63	V

5. Wi-Fi RF Specification

5.1 2.4GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description
WLAN Standard	IEEE 802.11b/g/n/ac, WiFi compliant
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)
Number of Channels	2.4GHz : Ch1 ~ Ch14
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11g/n : 64-QAM,16-QAM, QPSK, BPSK 802.11ac : 256-QAM, 64-QAM,16-QAM, QPSK, BPSK
Output Power	802.11b /CCK : 16 dBm ± 1.5 dB @ EVM ≤ -9dB
	802.11g /64-QAM(R=3/4) : 15 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11n /64-QAM(R=5/6) : 14 dBm ± 1.5 dB @ EVM ≤ -27dB
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -96 dBm, typical
	- 2Mbps PER @ -90 dBm, typical
	- 5.5Mbps PER @ -88 dBm, typical
	- 11Mbps PER @ -87 dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -90 dBm, typical
	- 9Mbps PER @ -88 dBm, typical
	- 12Mbps PER @ -87 dBm, typical
	- 18Mbps PER @ -85 dBm, typical
	- 24Mbps PER @ -83 dBm, typical
	- 36Mbps PER @ -80 dBm, typical
	- 48Mbps PER @ -76 dBm, typical
- 54Mbps PER @ -74 dBm, typical	
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -89 dBm, typical
	- MCS=1 PER @ -85 dBm, typical
	- MCS=2 PER @ -84 dBm, typical
	- MCS=3 PER @ -80 dBm, typical
	- MCS=4 PER @ -77 dBm, typical
	- MCS=5 PER @ -75 dBm, typical
	- MCS=6 PER @ -72 dBm, typical
- MCS=7 PER @ -71 dBm, typical	
Maximum Input Level	802.11b : -10dBm
	802.11g/n : -20dBm

Antenna Reference	Small antennas with 0~2 dBi peak gain
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5.1 5GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac, Wi-Fi compliant
Frequency Range	5.18 GHz ~ 5.845 GHz (5.0 GHz ISM Band)
Number of Channels	5.0GHz : Please see the table ¹
Modulation	802.11a/n : 64-QAM,16-QAM, QPSK, BPSK 802.11ac : 256-QAM, 64-QAM,16-QAM, QPSK, BPSK
Output Power	802.11a /64-QAM(R=3/4) : 14 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11n /64-QAM(R=5/6) : 13 dBm ± 1.5 dB @ EVM ≤ -27dB
	802.11ac/256-QAM(R=3/4) : 12 dBm ± 1.5 dB @ EVM ≤ -30dB
	802.11ac/256-QAM(R=5/6) : 10 dBm ± 1.5 dB @ EVM ≤ -32dB
Receive Sensitivity (11a, 20MHz) @10% PER	- 6Mbps PER @ -91 dBm, typical
	- 9Mbps PER @ -89 dBm, typical
	- 12Mbps PER @ -88 dBm, typical
	- 18Mbps PER @ -86 dBm, typical
	- 24Mbps PER @ -82 dBm, typical
	- 36Mbps PER @ -79 dBm, typical
	- 48Mbps PER @ -74 dBm, typical
	- 54Mbps PER @ -73 dBm, typical
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -90 dBm, typical
	- MCS=1 PER @ -88 dBm, typical
	- MCS=2 PER @ -85 dBm, typical
	- MCS=3 PER @ -82 dBm, typical
	- MCS=4 PER @ -78 dBm, typical
	- MCS=5 PER @ -74 dBm, typical
	- MCS=6 PER @ -72 dBm, typical
	- MCS=7 PER @ -71 dBm, typical

Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0	PER @ -88 dBm, typical
	- MCS=1	PER @ -85 dBm, typical
	- MCS=2	PER @ -83 dBm, typical
	- MCS=3	PER @ -79 dBm, typical
	- MCS=4	PER @ -76 dBm, typical
	- MCS=5	PER @ -71 dBm, typical
	- MCS=6	PER @ -70 dBm, typical
	- MCS=7	PER @ -68 dBm, typical
Receive Sensitivity (11ac,20MHz) @10% PER	- MCS=0	PER @ -89 dBm, typical
	- MCS=1	PER @ -87 dBm, typical
	- MCS=2	PER @ -84 dBm, typical
	- MCS=3	PER @ -81 dBm, typical
	- MCS=4	PER @ -77 dBm, typical
	- MCS=5	PER @ -73 dBm, typical
	- MCS=6	PER @ -71 dBm, typical
	- MCS=7	PER @ -70 dBm, typical
Receive Sensitivity (11ac,40MHz) @10% PER	- MCS=0	PER @ -87 dBm, typical
	- MCS=1	PER @ -83 dBm, typical
	- MCS=2	PER @ -81 dBm, typical
	- MCS=3	PER @ -78 dBm, typical
	- MCS=4	PER @ -75 dBm, typical
	- MCS=5	PER @ -70 dBm, typical
	- MCS=6	PER @ -68 dBm, typical
	- MCS=7	PER @ -66 dBm, typical
	- MCS=8	PER @ -64 dBm, typical
	- MCS=9	PER @ -63 dBm, typical
Receive Sensitivity (11ac,80MHz) @10% PER	- MCS=0	PER @ -83 dBm, typical
	- MCS=1	PER @ -80 dBm, typical
	- MCS=2	PER @ -78 dBm, typical
	- MCS=3	PER @ -74 dBm, typical
	- MCS=4	PER @ -71 dBm, typical
	- MCS=5	PER @ -69 dBm, typical
	- MCS=6	PER @ -65 dBm, typical
	- MCS=7	PER @ -63 dBm, typical
	- MCS=8	PER @ -60 dBm, typical
	- MCS=9	PER @ -59 dBm, typical

Maximum Input Level	802.11a/n : -20dBm
	802.11ac : -30dBm
Antenna Reference	Small antennas with 0~2 dBi peak gain

¹5GHz Channel table

Band (GHz)	Operating Channel Numbers	Channel center frequencies(MHz)
5.15GHz~5.25GHz	36	5180
	40	5200
	44	5220
	48	5240
5.25GHz~5.35GHz	52	5260
	56	5280
	60	5300
	64	5320
5.5GHz~5.7GHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640
	132	5660
	136	5680
5.725GHz~5.825GHz	140	5700
	149	5745
	153	5765
	157	5785
	161	5805

6. Bluetooth Specification

6.1 Bluetooth Specification

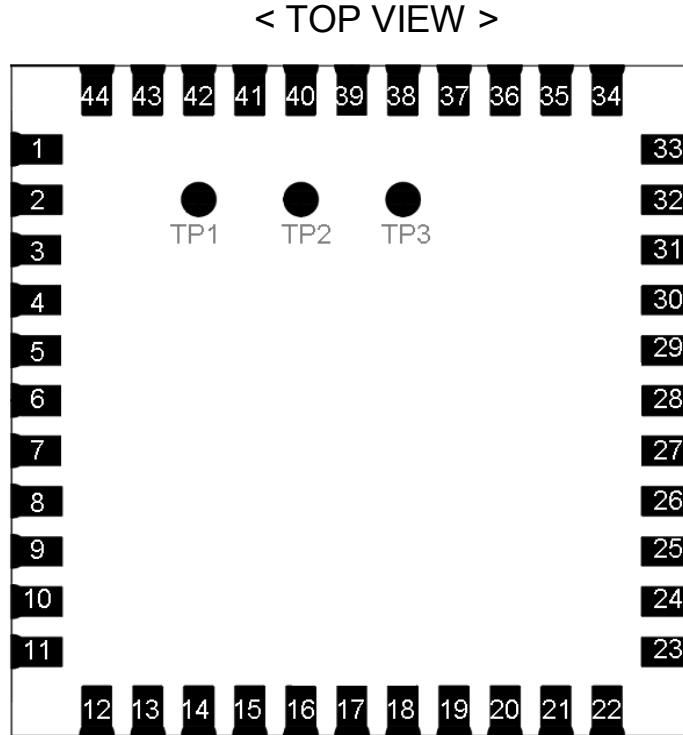
Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V4.2 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	FHSS, GFSK, DPSK, DQPSK		
RF Specification			
	Min.	Typical.	Max.
Output Power¹	0	-	10
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80 dBm	
Maximum Input Level	GFSK (1Mbps) :-20dBm		
	$\pi/4$ -DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

NOTE¹ : Output power can be configured by HCD firmware.

7. Pin Assignments

7.1 Pin Outline



7.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	NC	—	Floating (Don't connected to ground)
5	NC	—	Floating (Don't connected to ground)
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	NC	—	Floating (Don't connected to ground)
9	VBAT	P	Main power voltage source input
10	XTAL_IN	I	Crystal input
11	XTAL_OUT	O	Crystal output
12	WL_REG_ON	I	Power up/down internal regulators used by WiFi section
13	WL_HOST_WAKE	O	WLAN to wake-up HOST

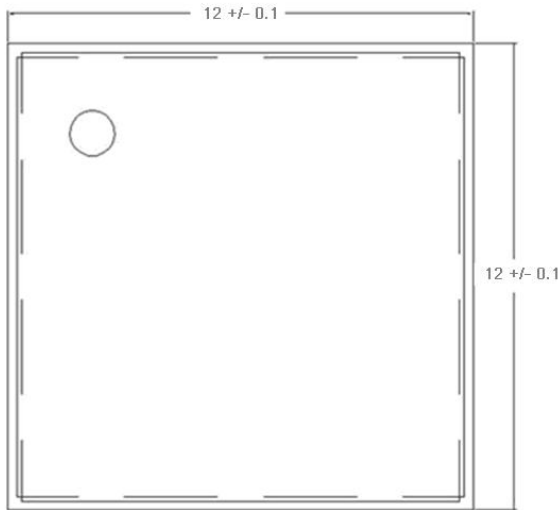
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	External Low Power Clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	SDIO_VSEL	I/O	SDIO mode selection pin
30	NC	—	Floating (Don't connected to ground)
31	GND	—	Ground connections
32	NC	—	Floating (Don't connected to ground)
33	GND	—	Ground connections
34	BT_REG_ON	I	Power up/down internal regulators used by BT section
35	NC	—	Floating (Don't connected to ground)
36	GND	—	Ground connections
37	GPIO_6	I/O	GPIO configuration pin
38	GPIO_3	I/O	GPIO configuration pin
39	GPIO_5	I/O	GPIO configuration pin
40	GPIO_2	I/O	GPIO configuration pin
41	UART_RTS_N	O	Bluetooth UART interface
42	UART_TXD	O	Bluetooth UART interface
43	UART_RXD	I	Bluetooth UART interface
44	UART_CTS_N	I	Bluetooth UART interface
45	TP1(NC)	—	Floating (Don't connected to ground)
46	TP2(NC)	—	Floating (Don't connected to ground)
47	TP3(NC)	—	Floating (Don't connected to ground)

8. Dimensions

8.1 Physical Dimensions

(Unit: mm)

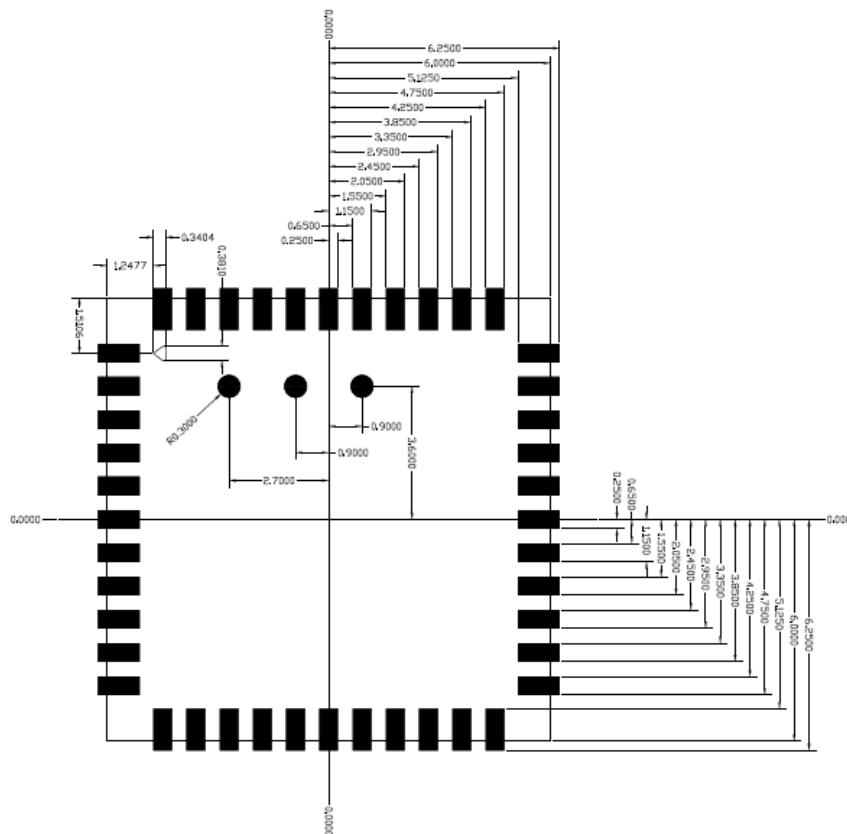
< TOP VIEW >



< Side View >



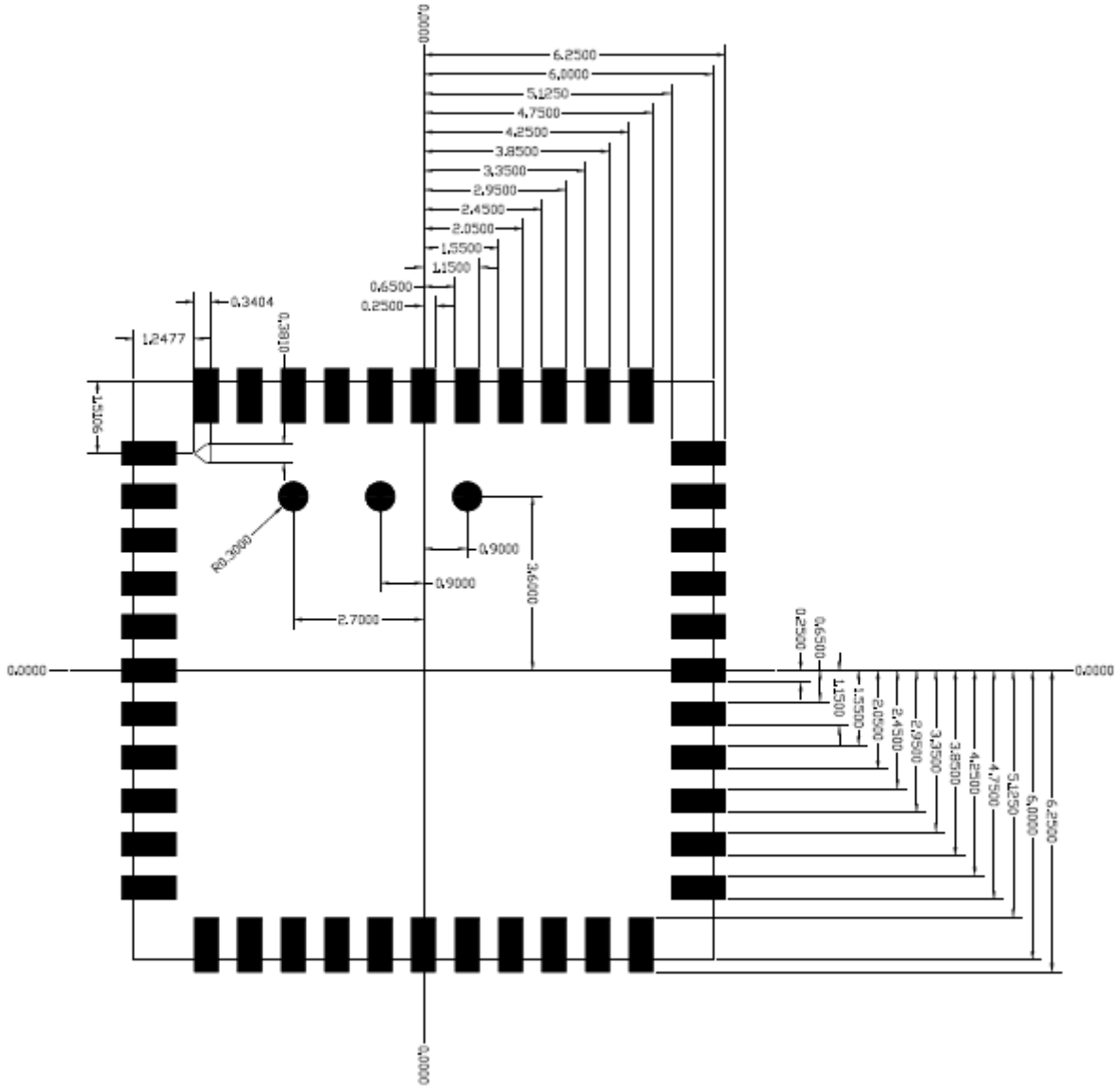
< TOP VIEW >



8.2 Layout Recommendation

(Unit: mm)

< TOP VIEW >



9. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	± 30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

10.1 SDIO Pin Description

All three package options of the WLAN section provide support for SDIO version 3.0 including the new UHS-I modes:

- DS: Default speed up to 25MHz (3.3V signaling).
- HS: High speed up to 50MH (3.3V signaling).
- SDR12: SDR up to 25MHz (1.8V signaling).
- SDR25: SDR up to 50MHz (1.8V signaling).
- SDR50: SDR up to 100MHz (1.8V signaling).
- SDR104: SDR up to 208MHz (1.8V signaling).
- DDR50: DDR up to 50MHz (1.8V signaling).

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by SDIO interface. The ability to force control of gated clocks from within the device is also provided.

The following three functions are supported:

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

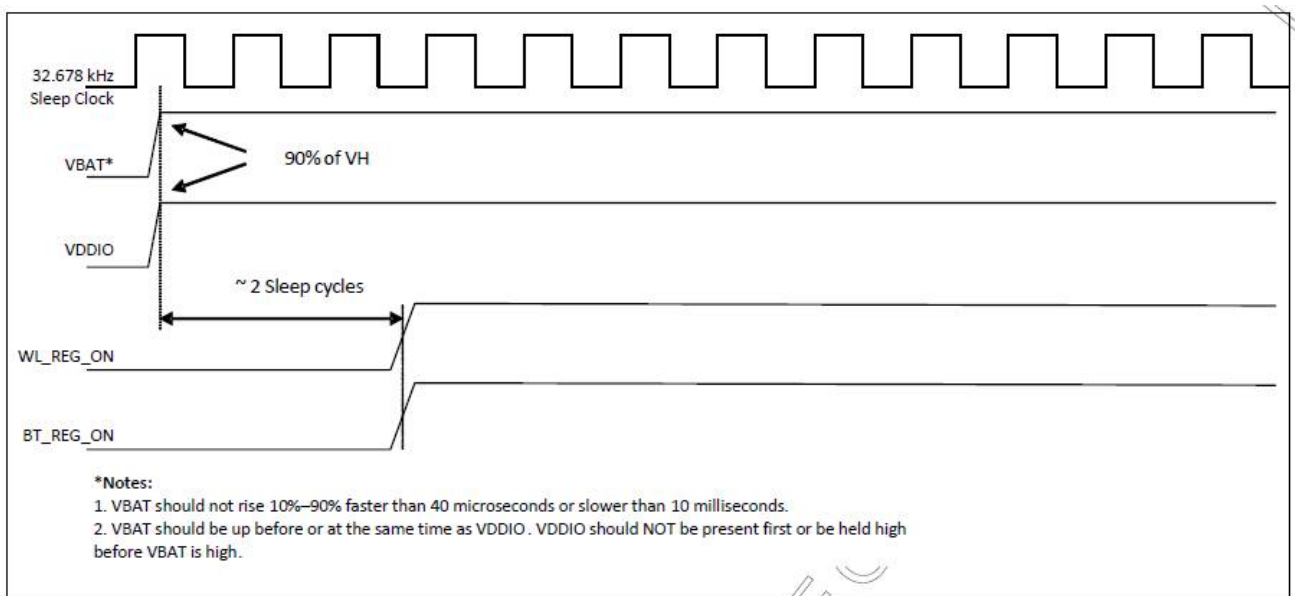
10. Host Interface Timing Diagram

10.1 Power-up Sequence Timing Diagram

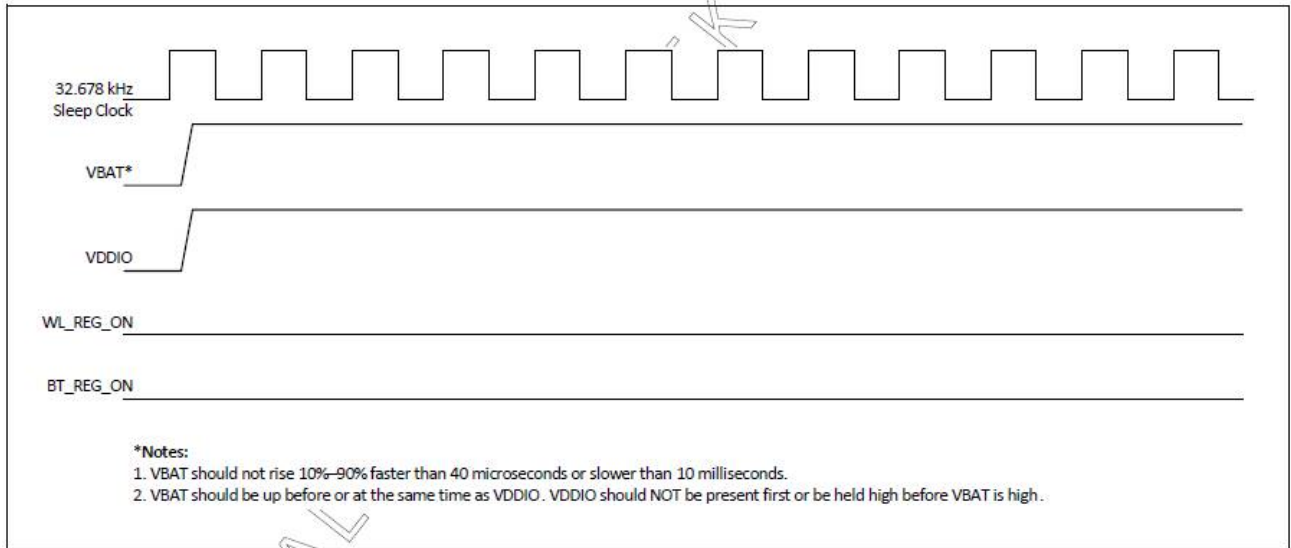
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

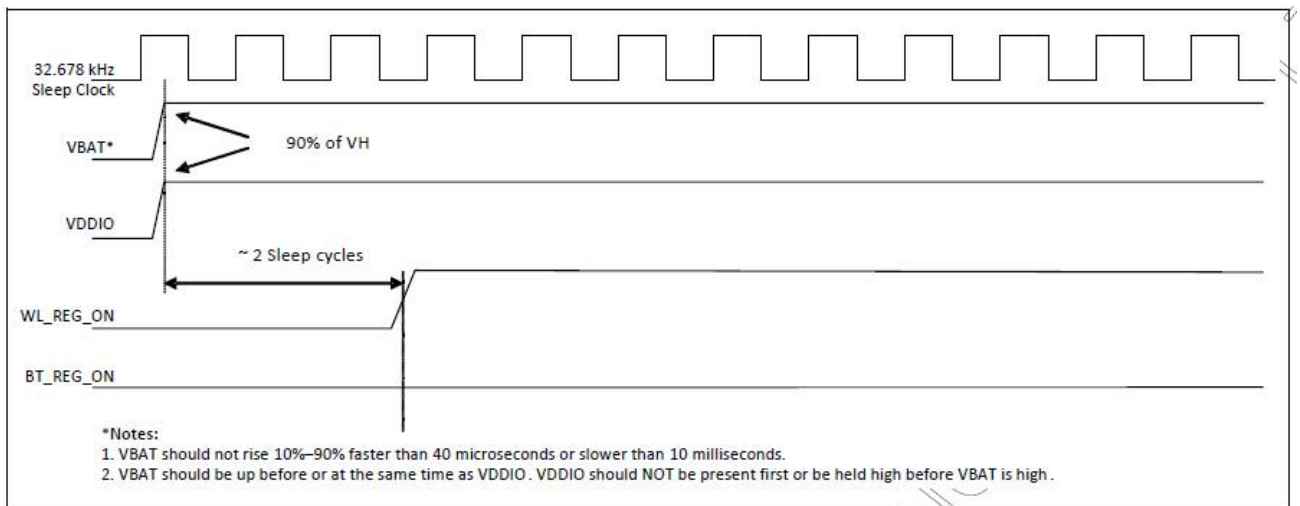
- ※ WL_REG_ON: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- ※ BT_REG_ON: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



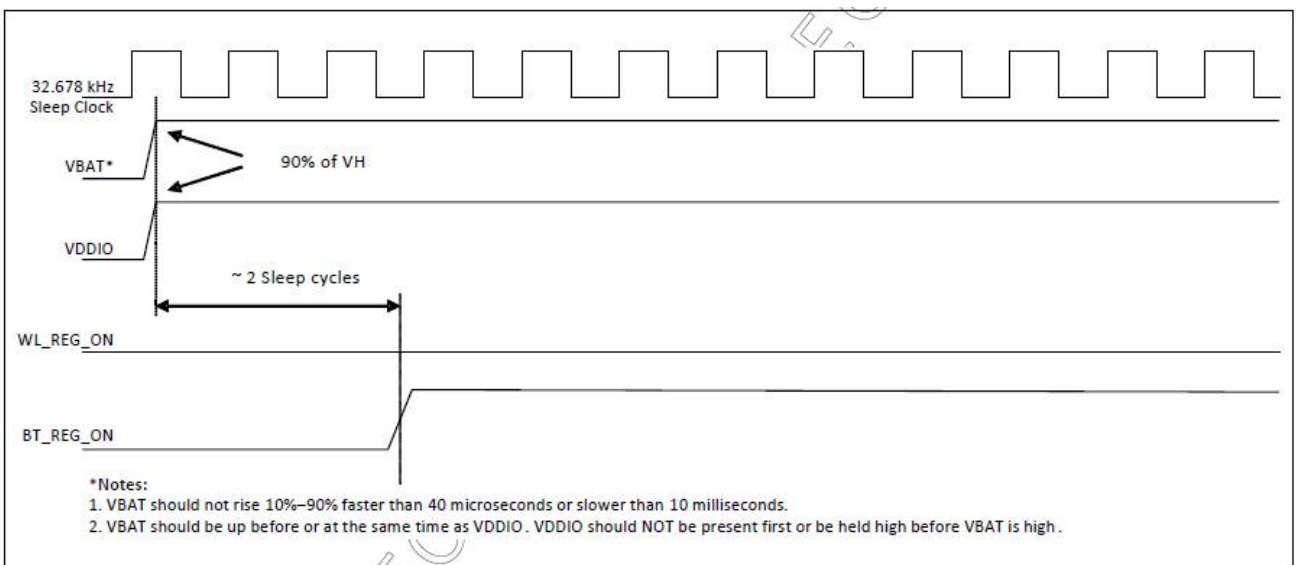
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

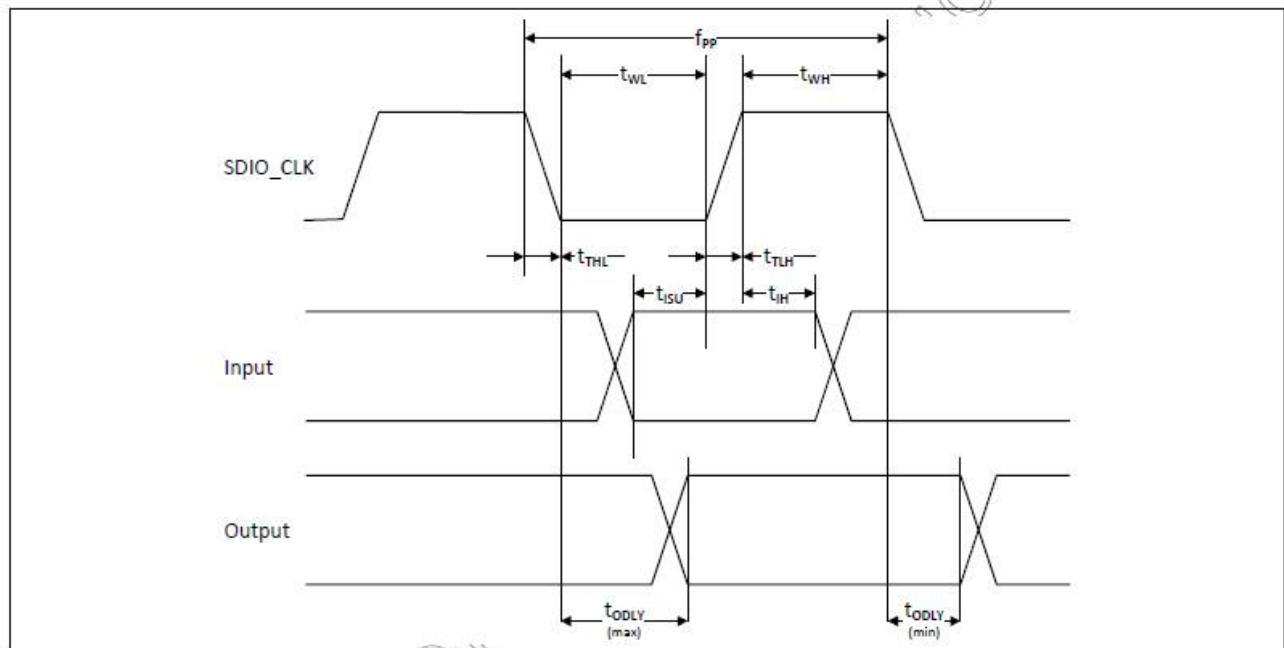


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

10.2 SDIO Default Mode Timing Diagram

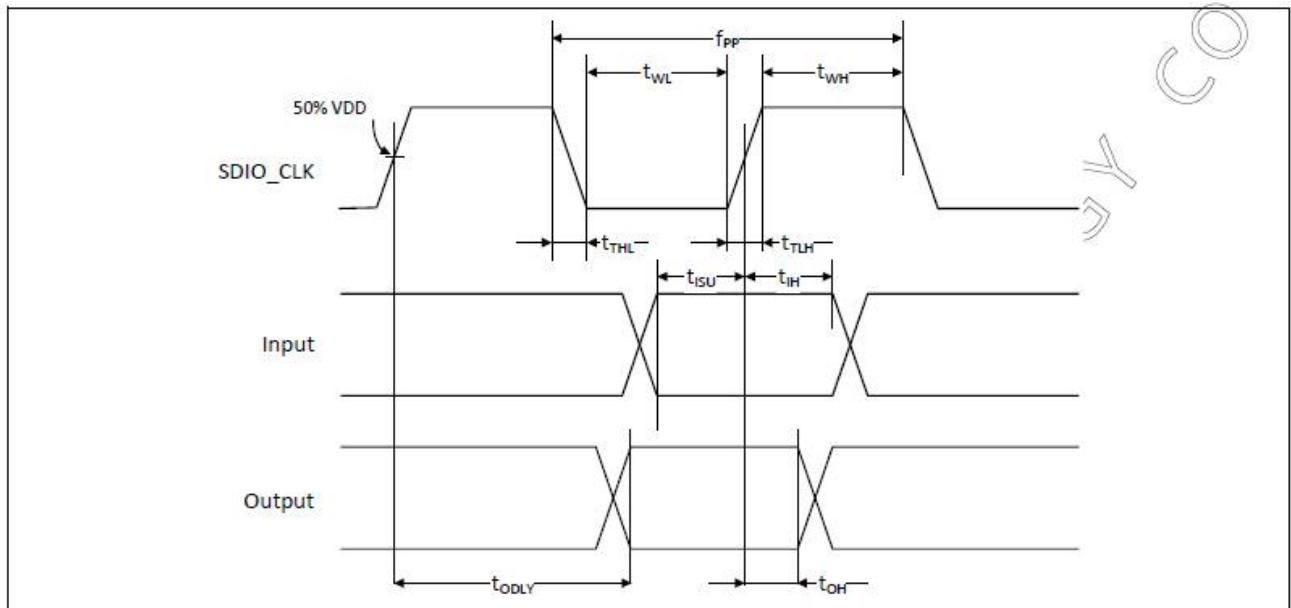


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^b)					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTLL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on $CL \leq 40\text{pF}$ load on CMD and Data.

b. $\min(V_{ih}) = 0.7 \times V_{DDIO}$ and $\max(V_{il}) = 0.2 \times V_{DDIO}$.

10.3 SDIO High Speed Mode Timing Diagram

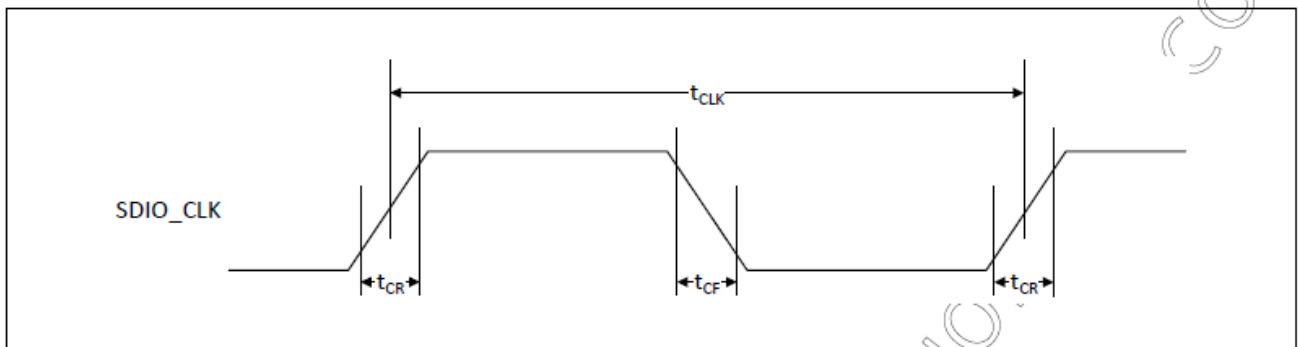


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on $CL \leq 40$ pF load on CMD and Data.
 b. $\min(V_{ih}) = 0.7 \times V_{DDIO}$ and $\max(V_{il}) = 0.2 \times V_{DDIO}$.

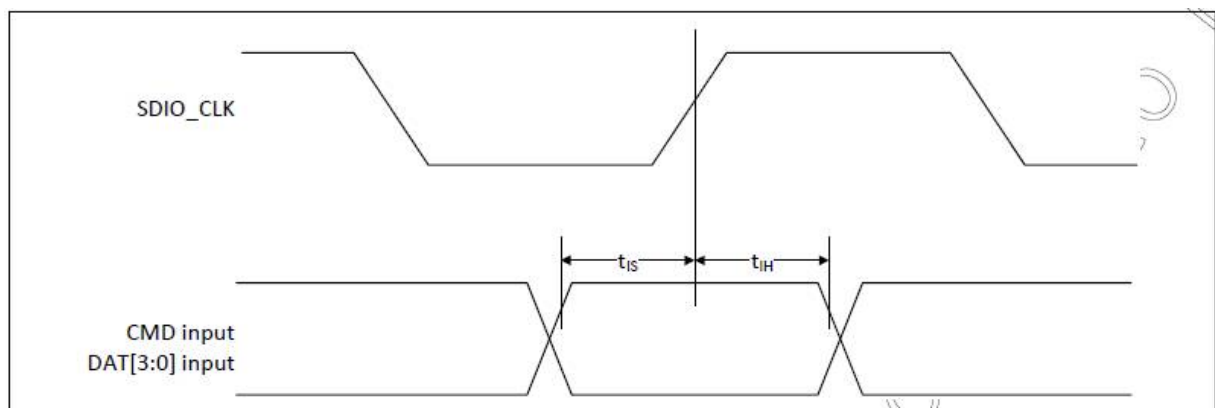
10.4 SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes)



Parameter	Symbol	Minimum	Maximum	Unit	Comments
-	t_{CLK}	40	-	ns	SDR12 mode
		20	-	ns	SDR25 mode
		10	-	ns	SDR50 mode
		4.8	-	ns	SDR104 mode
-	t_{CR}, t_{CF}	-	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (max) @100 MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max) @208 MHz, $C_{CARD} = 10$ pF
Clock duty	-	30	70	%	-

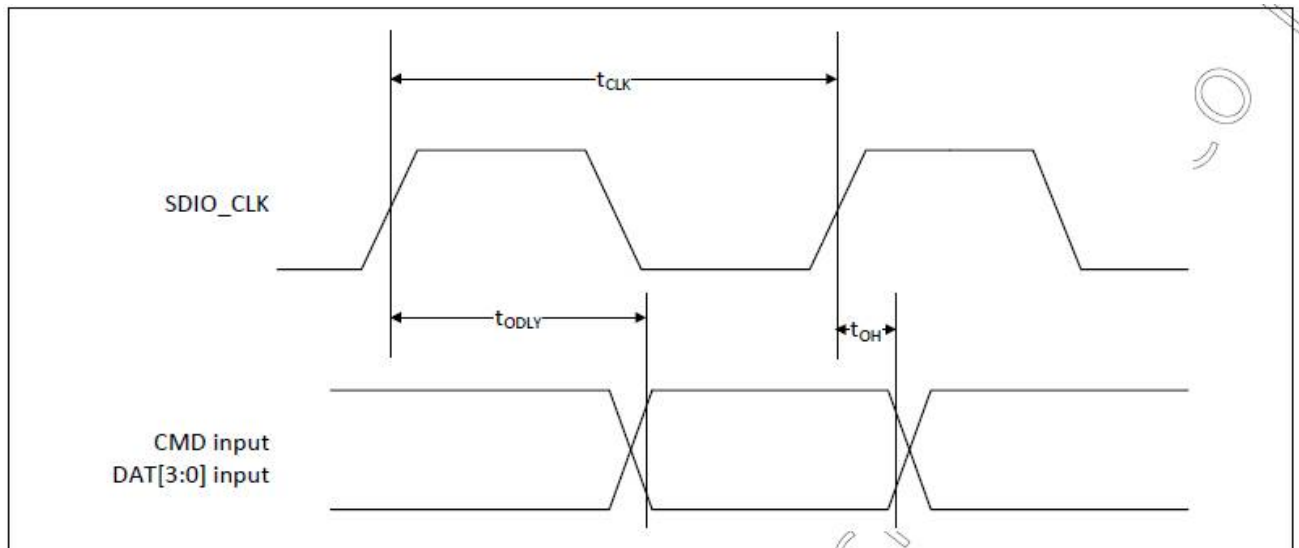
Card Input timing (SDR Modes)



Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.70 ^a	-	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	-	ns	$C_{CARD} = 5$ pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	-	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	-	ns	$C_{CARD} = 5$ pF, VCT = 0.975V

a. SDIO 3.0 specification value is 1.40 ns.

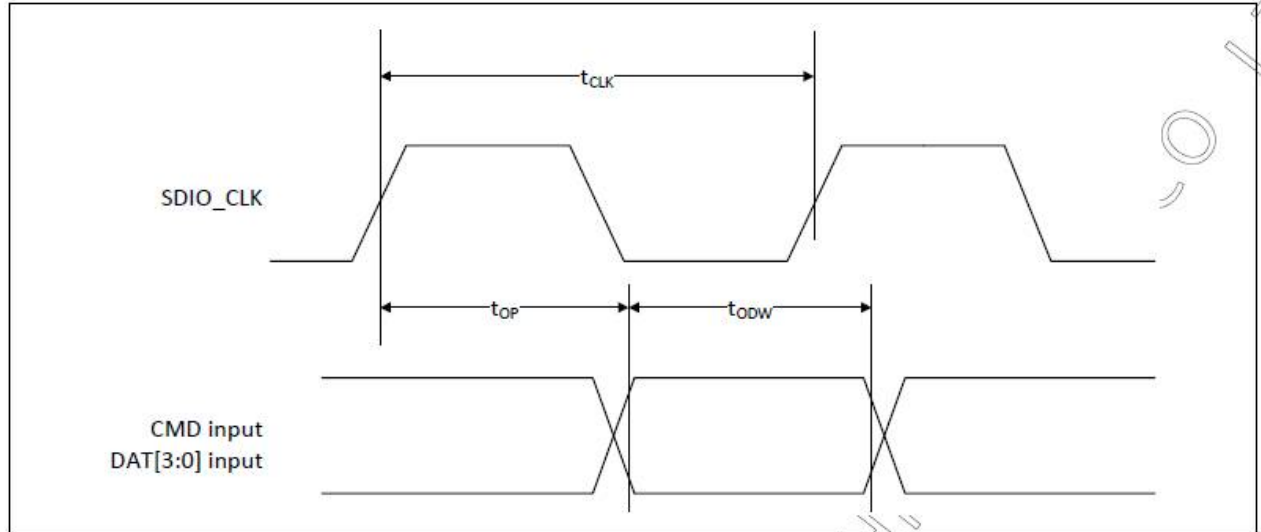
Card output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.85 ^a	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

a. SDIO 3.0 specification value is 7.5 ns.

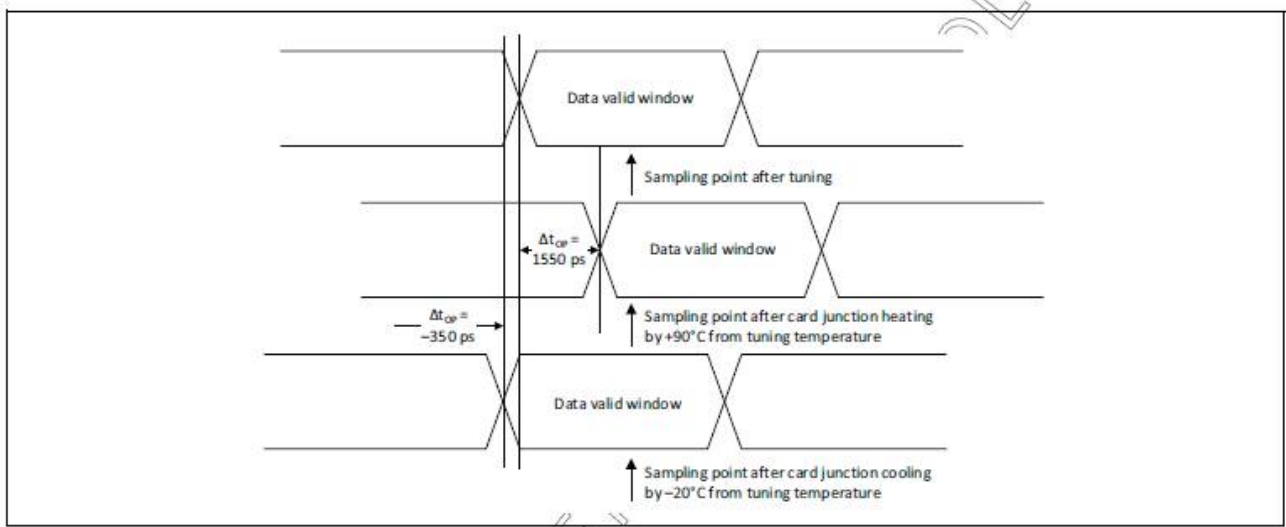
Card output timing (SDR Modes 100MHz to 208MHz)



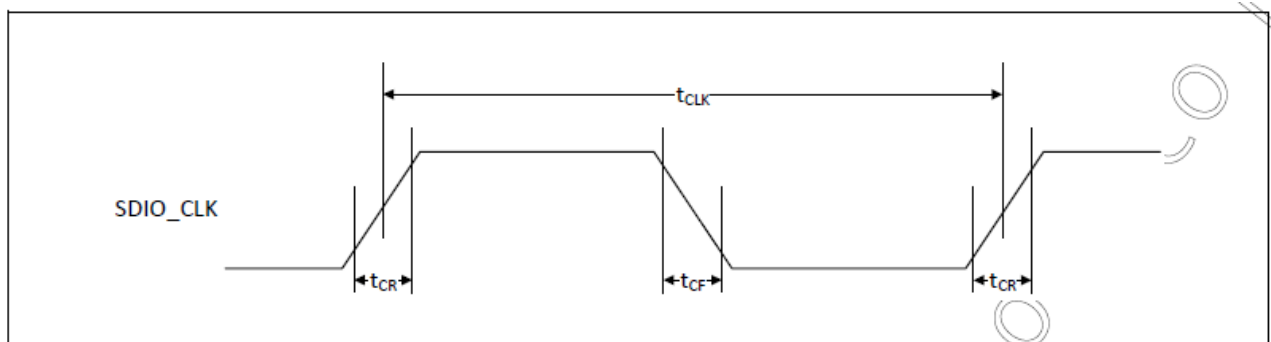
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	$t_{ODW} = 2.88$ ns @208 MHz

- $\Delta t_{OP} = +1550$ ps for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350$ ps for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600$ ps for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

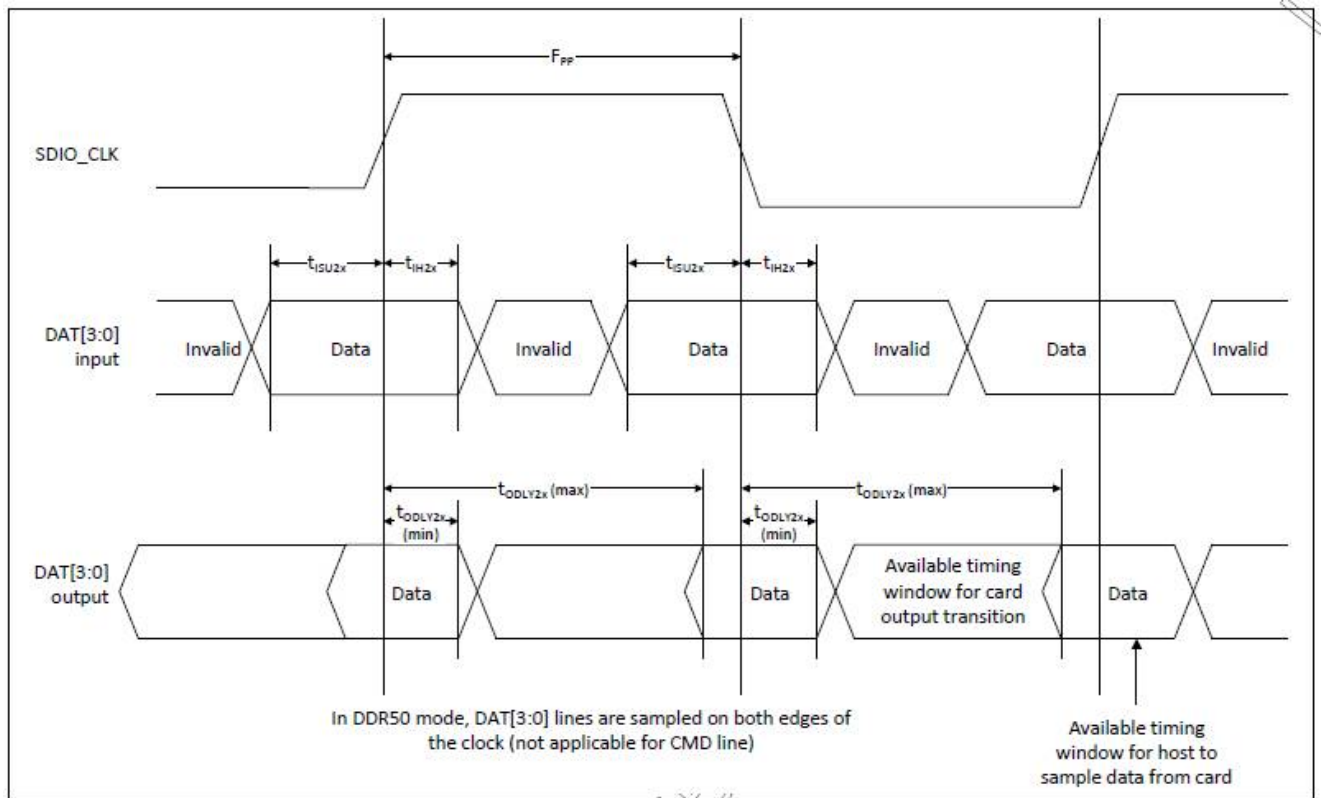


10.5 SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
-	t_{CLK}	20	-	ns	DDR50 mode
-	t_{CR}, t_{CF}	-	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00$ ns (max) @50 MHz, $C_{CARD} = 10$ pF
Clock duty	-	45	55	%	-

Data Timing



Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	–	ns	$C_{CARD} < 10\text{pF}$ (1 Card)
Input hold time	t_{IH}	0.8	–	ns	$C_{CARD} < 10\text{pF}$ (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	$C_{CARD} < 30\text{pF}$ (1 Card)
Output hold time	t_{OH}	1.5	–	ns	$C_{CARD} < 15\text{pF}$ (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	$C_{CARD} < 10\text{pF}$ (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	$C_{CARD} < 10\text{pF}$ (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.85 ^a	ns	$C_{CARD} < 25\text{pF}$ (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	$C_{CARD} < 15\text{pF}$ (1 Card)

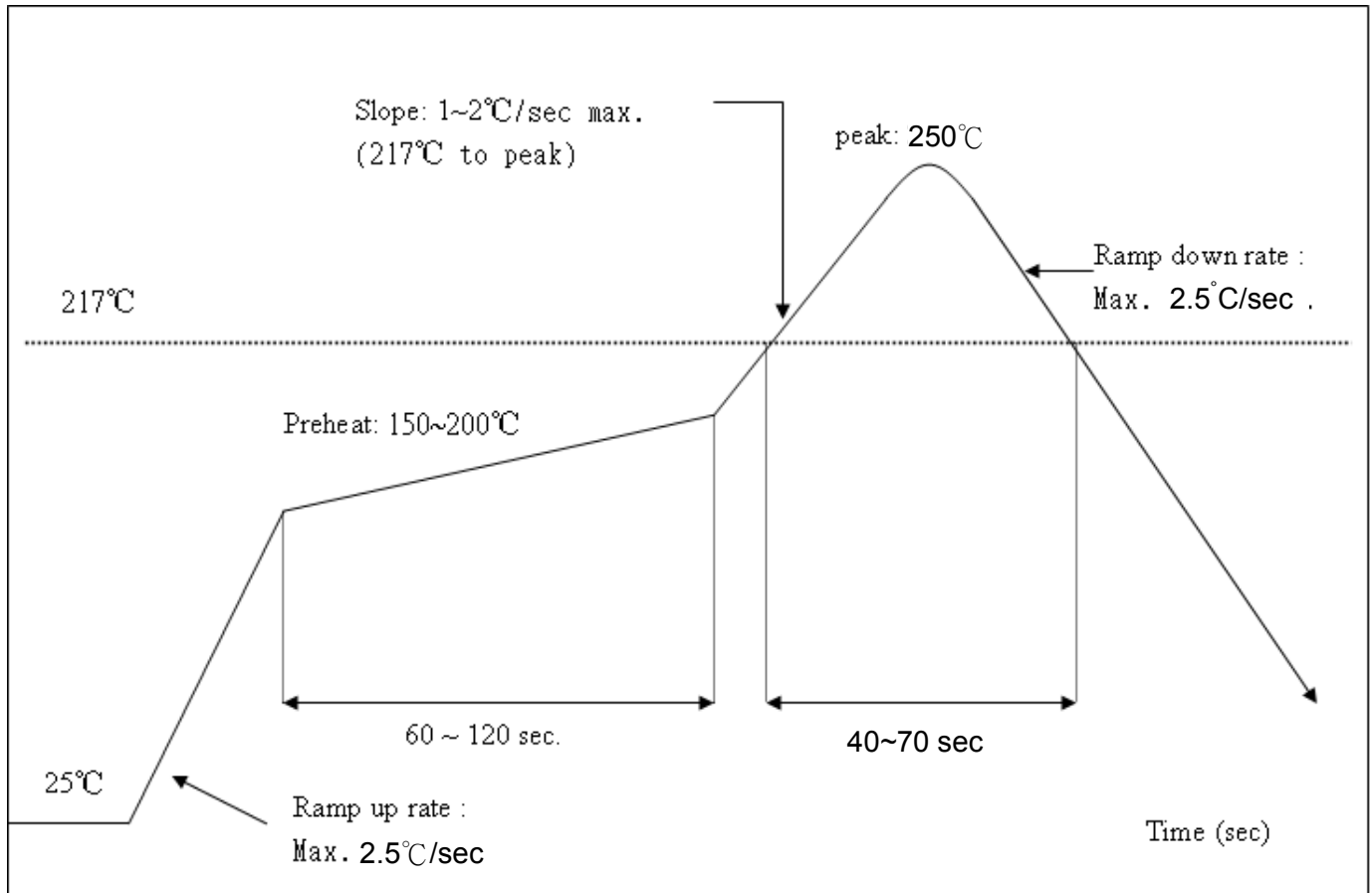
a. SDIO 3.0 specification value is 7.0 ns.

11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <math><250^{\circ}\text{C}</math>

Number of Times : ≤ 2 times

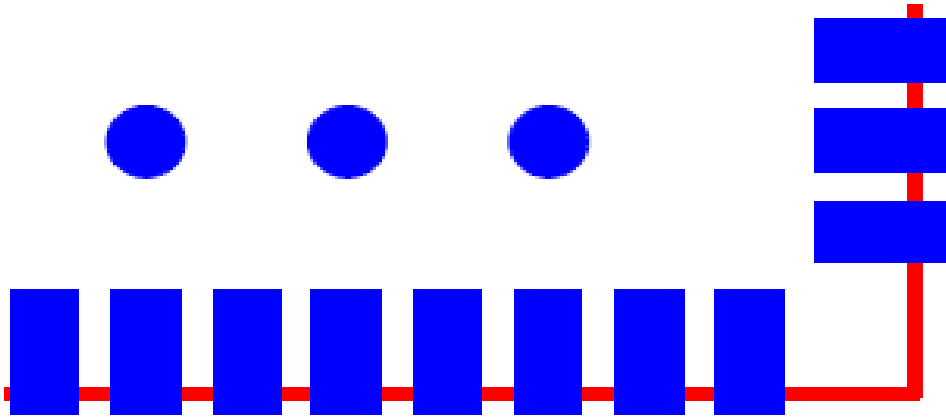


The notification of WiFi module before mounting:

The aperture of stencil should be larger than foot print of module, and the stencil thickness should be not less than 0.12mm.

Reflow 時需使用 N2, 含氧量建議 5000 ppm 以下,

It must use N2 for reflow and suggest the concentration of oxygen less than 5000 ppm .



模組規格 L 0.7mm

PCB Pad 設計 L 0.8mm

鋼網開孔建議 L0.5mm~0.6mm

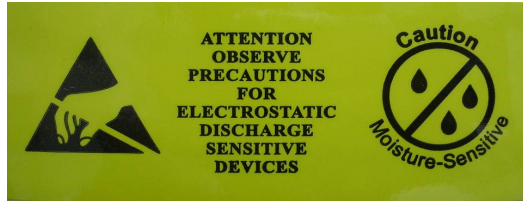
適當內縮可以避免撐高造成高度影響

- Module Specifications L 0.7mm
- The design for PCB Pad : L:0.8mm
- We recommend the apertures for stencil L:0.5mm~0.6mm
- In order to avoid highness impact caused solder paste thickness, the stencil open size can be appropriately retracted


12. Package Information

12.1 Label

Label A → Anti-static and humidity notice










Label B → MSL caution / Storage Condition

	Caution This bag contains MOISTURE-SENSITIVE DEVICES	LEVEL <input type="text"/>
	<small>If blank, see adjacent bar code label</small>	
<ol style="list-style-type: none"> 1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH) 2. Peak package body temperature: _____ °C <small>If blank, see adjacent bar code label</small> 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be <ol style="list-style-type: none"> a) Mounted within: _____ hours of factory conditions <small>If blank, see adjacent bar code label</small> ≤30°C/60% RH, or b) Stored per J-STD-033 4. Devices require bake, before mounting, if: <ol style="list-style-type: none"> a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C b) 3a or 3b are not met 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure 		
Bag Seal Date: _____ <small>If blank, see adjacent bar code label</small>		
<small>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</small>		

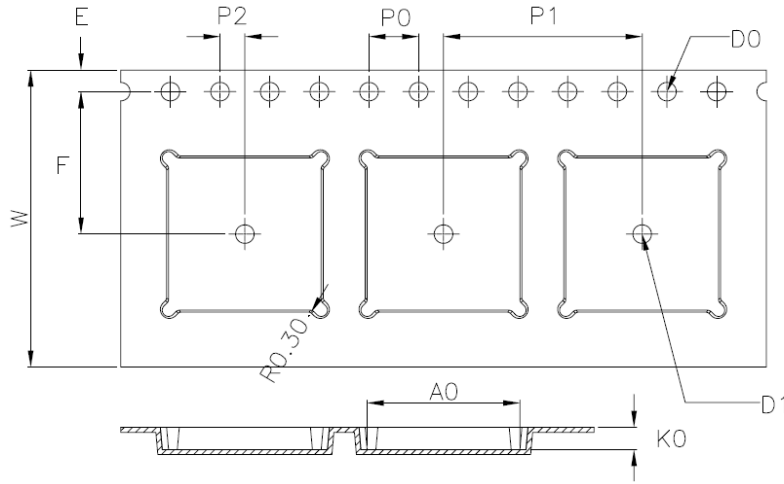
Label C → Inner box label .

PO:	
AMK DEVICE:	
PKG S/N:	 9PKGXXXXXXXXXX
Model :	 AP6XXX(HF)
P/N:	 99P-W01-0XXXR
Qty :	 1500
Date Code :	 XXXX
Lot Code :	 TXXXXXX

Label D → Carton box label .

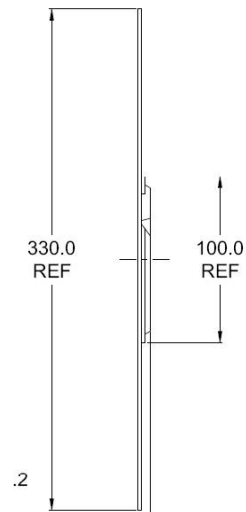
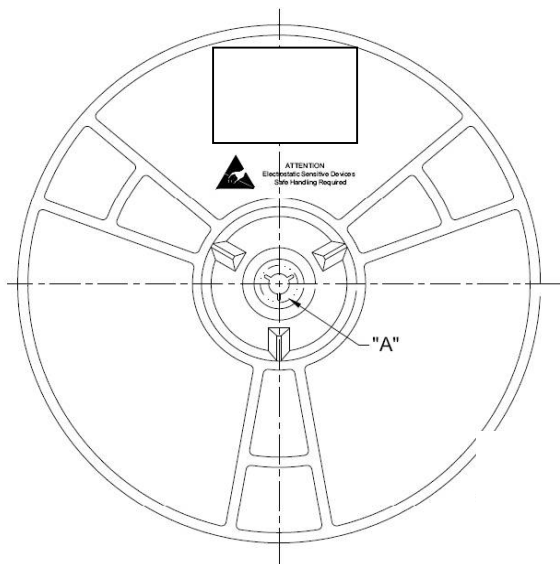
AMPAK Technology	
PO :	
AMK DEVICE:	
Model Name :	 AP6XXX (HF)
Part No.:	 99P-W01-0XXXR
Quantity :	 7500
Lot D/C:	 TXXXXXX XXXX
Manufacture:	 YYYY/MM/DD

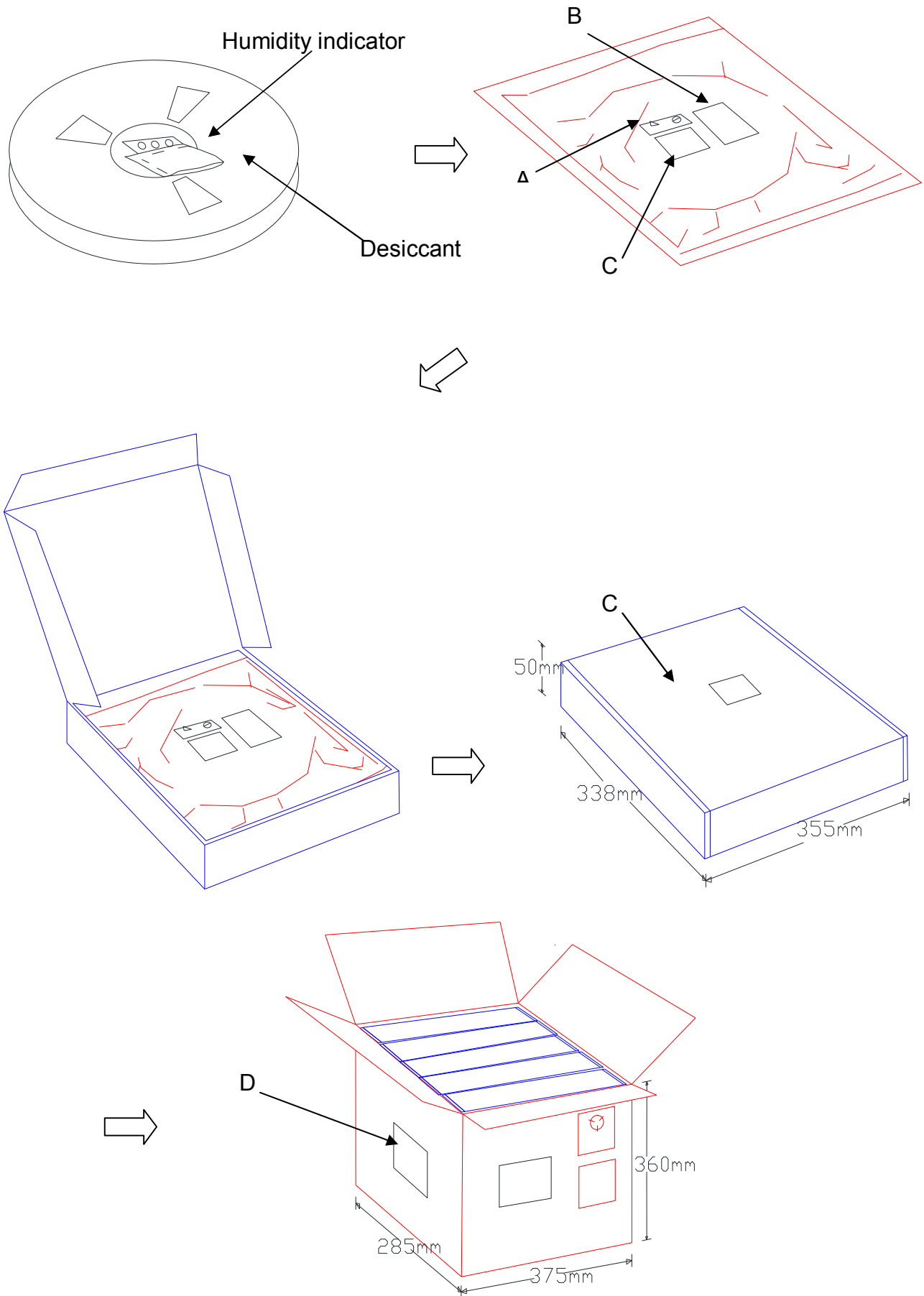
12.2 Dimension




W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 ^{+0.10} / _{-0.00}
D1	∅1.50MIN

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.





12.3 MSL Level / Storage Condition

	<p>Caution This bag contains MOISTURE-SENSITIVE DEVICES</p>	<p>LEVEL 4</p> <p><small>If blank, see adjacent bar code label</small></p>
<p>1. Calculated shelf life in sealed bag: 12 months at <math><40^{\circ}\text{C}</math> and <math><90\%</math> relative humidity (RH)</p>		
<p>2. Peak package body temperature: <u>250</u> $^{\circ}\text{C}$ <small>If blank, see adjacent bar code label</small></p>		
<p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be</p>		
<p>a) Mounted within: <u>72</u> hours of factory conditions <small>If blank, see adjacent bar code label</small></p> <p style="padding-left: 40px;">$\leq 30^{\circ}\text{C}/60\% \text{ RH, or}$</p>		
<p>b) Stored per J-STD-033</p>		
<p>4. Devices require bake, before mounting, if:</p>		
<p>a) Humidity Indicator Card reads >10% for level 2a-5a devices or >60% for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$</p>		
<p>b) 3a or 3b are not met.</p>		
<p>5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.</p>		
<p>Bag Seal Date: _____ <small>If blank, see adjacent bar code label</small></p>		
<p>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p>		

※NOTE : Accumulated baking time should not exceed 96hrs