AzureWave Technologies, Inc.

AW-AM497

IEEE 802.11 a/b/g/n Wi-Fi with ac friendly + Bluetooth 5.0 Combo LGA Module

Datasheet

Rev. E

DF

(For Standard)

Features

WLAN

- Full IEEE 802.11a/b/g/n compatibility with enhanced performance:
- 802.11ac friendly, MCS8 (256-QAM) for 20 MHz channels in 5 GHz band.
- Single spatial stream with PHY data rates of up to 72.2 Mbps with 802.11n (MCS7) and 78 Mbps with 802.11ac (MCS8).
- 20 MHz channels with optional SGI support for MCS0-MCS7.
- IEEE 802.11ac explicit beamformer support.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Receive space-time block coding (STBC)
- On-chip power amplifier/low-noise amplifier for both bands.

Bluetooth

- All optional Bluetooth 4.2 features supported.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports BDR (1Mbps), EDR (2/3Mbps), BLE (1/2Mbps).
- Host controller interface (HCI) using a high-speed UART interface.
- PCM for audio data.
- Bluetooth 5.0 compliant with 2 Mbps GFSK data rate for BLE.

AzureWave Technologies, Inc.

Revision History

Document NO: **R2-2497-DST-01**

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/07/27	DCN018259	● First Release	QM.TAN	N.C Chen
B	2021/01/26	DCN020584	● Re-format	QM.TAN	N.C Chen
C	2021/04/13	DCN021225	● Cypress to Infineon ● Update ESD Specification ● Modify BT Rx Specification	QM.TAN	N.C Chen
D	2021/06/18	DCN022113	● Update Power Consumption ● Update ESD Specification	QM.TAN	N.C Chen
E	2021/08/19	DCN022947	● Update Pin Out	QM.TAN	N.C Chen

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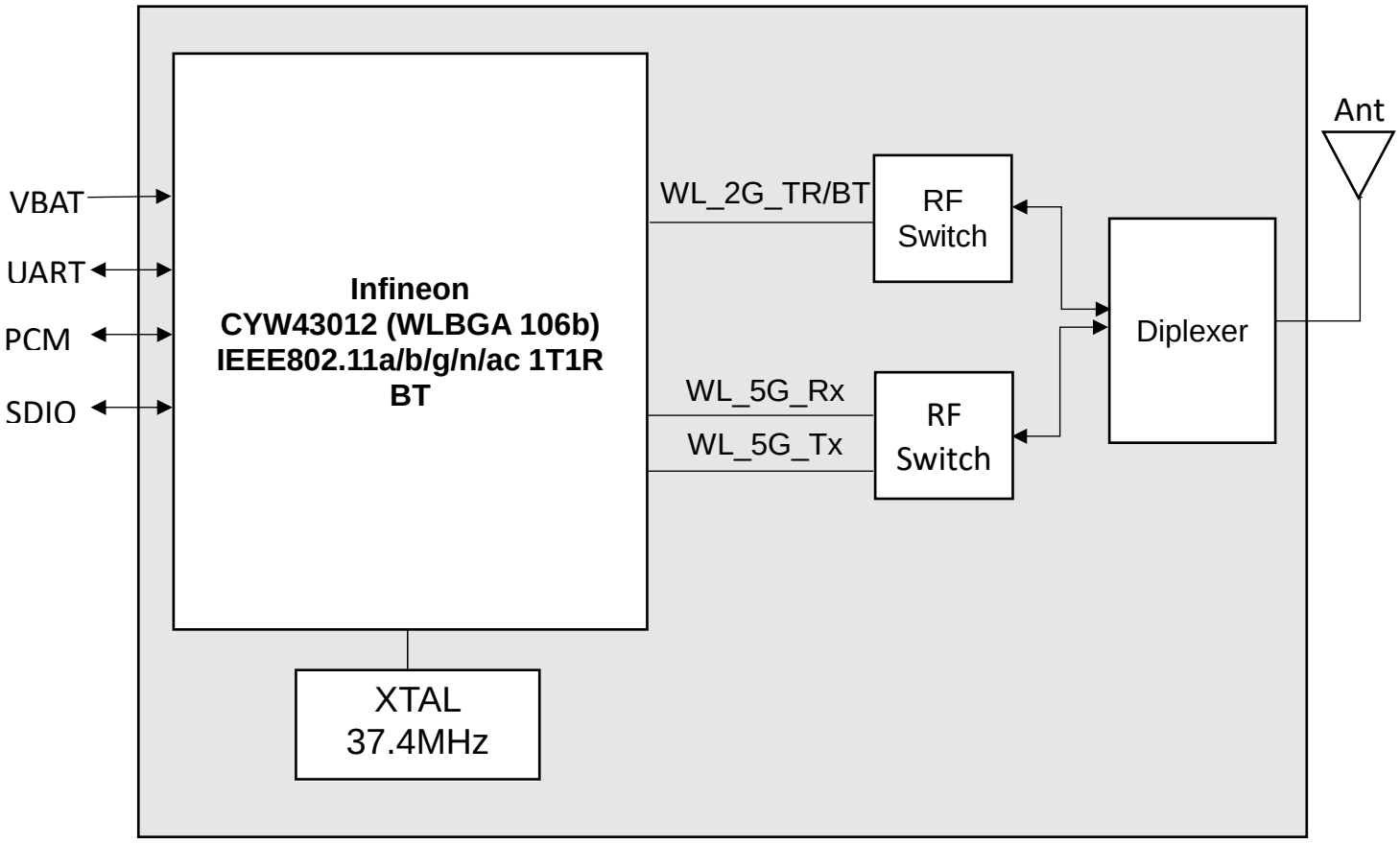
Table of Contents

1. Introduction

1.1 Product Overview

The Infineon CYW43012 single-chip device integrates a IEEE 802.11a/b/g/n compliant 802.11ac-friendly MAC/baseband/radio and Bluetooth 5.0 + EDR (enhanced data rate). It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly mobile devices that require minimal power consumption and reliable operation.

1.2 Block Diagram



AW-AM497 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n Wi-Fi with ac friendly + Bluetooth 5.0 Combo LGA Module
Major Chipset	CYW43012 (WLBGA 106p)
Host Interface	WiFi + BT ● SDIO + UART
Dimension	12.0mm(L) x 12.0mm(W) x 1.75 mm(H)
Form Factor	● LGA module, 47 pins
Antenna	For LGA, “1T1R, external” ANT1(Main)：WiFi/Bluetooth → TX/RX
Weight	0.5g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE802.11 a/b/g/n/ac 1T1R
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	802.11a/g/n/ac: OFDM 802.11b: CCK(11, 5.5Mbps), DQPSK(2Mbps), BPSK(1Mbps)
Number of Channels	802.11b: USA, Canada and Taiwan – 1 ~ 11 Most European Countries – 1 ~ 13 802.11g: USA and Canada – 1 ~ 11 Most European Countries – 1 ~ 13 802.11n:

<table>
<tr><td></td><td>USA and Canada – 1 ~ 11
Most European Countries – 1 ~ 13
802.11a:
USA – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165</td></tr>
<tr><td>Output Power (Board Level Limit)*</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps) @EVM<35%</td><td>16</td><td>18</td><td>20</td><td>dBm</td></tr>
<tr><td>11g (54Mbps) @EVM≦-25 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-27 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps) @EVM≦-25 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-27 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11ac (VHT20 MCS8) @EVM≦-30 dB</td><td>8</td><td>10</td><td>12</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>-89</td><td>-86</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>-77</td><td>-74</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-77</td><td>-74</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>-75</td><td>-72</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-75</td><td>-72</td><td>dBm</td></tr>
<tr><td>11ac (VHT20 MCS8)</td><td>-</td><td>-72</td><td>-69</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Data Rate</td><td>802.11b: 1, 2, 5.5, 11Mbps
802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n:MCS0~7
802.11ac:MCS0~8</td></tr>
<tr><td>Security</td><td>◆ WEP</td></tr>
</table>

	◆ WPA Personal, WPA2 Personal, WPA3 Personal ◆ WMM, WMM-PS (U-APSD), WMM-SA, AES (hardware accelerator) ◆ TKIP (hardware accelerator) ◆ CKIP (software support)

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

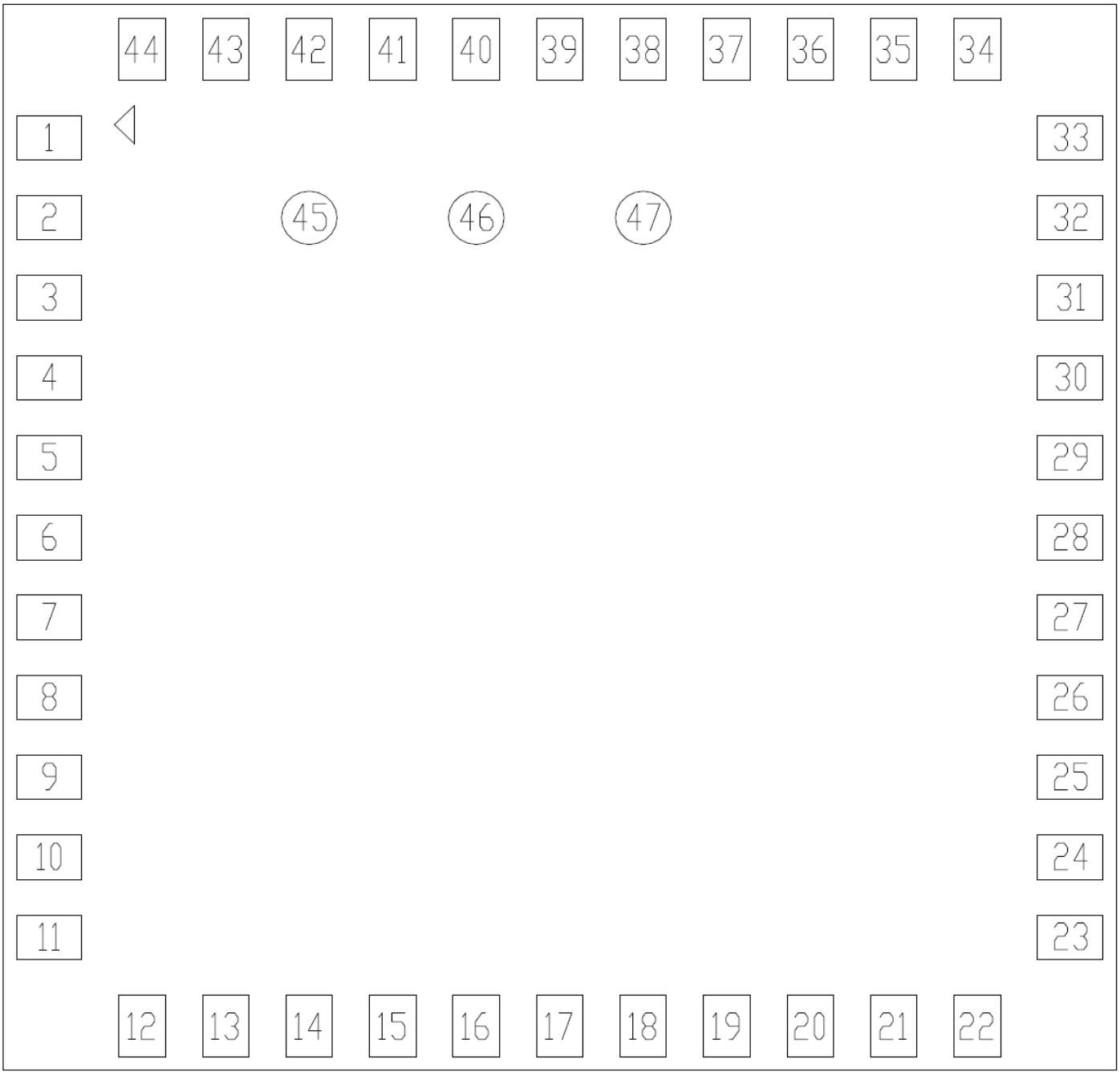
<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 5.0</td></tr>
<tr><td>Bluetooth VID/PID</td><td>N/A</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2480MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK
Payload 2M: 4-DQPSK
Payload 3M: 8DPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>Basic Rate</td><td>6</td><td>8</td><td>10</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>6</td><td>8</td><td>10</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>BT Sensitivity (BER<0.1%)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td></td><td>-92</td><td>-87</td><td>dBm</td></tr>
<tr><td>EDR (2DH5)</td><td></td><td>-92</td><td>-87</td><td>dBm</td></tr>
<tr><td>EDR (3DH5)</td><td></td><td>-87</td><td>-82</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td></td><td>-95</td><td>-90</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	VBAT: 3.2~4.4V VIO : 1.8V
Operating Temperature	-20℃ to +70℃
Operating Humidity	less than 85% R.H.
Storage Temperature	-40℃ to +125℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	1.5KV per MIL-STD-883H Method 3015.8
Changed Device Model	500V per JEDEC EIA/JESD22-C101E

2. Pin Definition

2.1 Pin Map



AW-AM497 Pin Map (Top View)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND1	Ground.		GND
2	WL_BT_ANT	WLAN/BT RF TX/RX path.		RF
3	GND2	Ground.		GND
4	NC1	Floating		I/O
5	NC2	Floating		I/O
6	BT_WAKE	BT Device Wake		I
7	BT_HOST_WAKE	BT Host Wake		O
8	CLK_REQ	Reference clock request		I/O
9	VBAT	3.3V power pin	3.3V	VCC
10	NC3	Floating		I
11	NC4	Floating		O
12	WL_REG_ON	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.		I
13	WL_HOST_WAKE	WL Host Wake		O
14	SDIO_DATA_2	SDIO Data Line 2		I/O
15	SDIO_DATA_3	SDIO Data Line 3		I/O
16	SDIO_CMD	SDIO Command Input		I/O
17	SDIO_CLK	SDIO Clock		I
18	SDIO_DATA_0	SDIO Data Line 0		I/O
19	SDIO_DATA_1	SDIO Data Line 1		I/O
20	GND3	Ground.		GND
21	VIN_LDO_OUT	Internal Buck voltage generation pin		VCC
22	VDDIO	1.8V VDDIO supply for WLAN and BT	1.8V	VCC
23	VIN_LDO	Internal Buck voltage generation pin		VCC
24	LPO	External 32K or RTG clock		I
25	PCM_OUT	PCM data out		O
26	PCM_CLK	PCM clock		I/O
27	PCM_IN	PCM data input		I
28	PCM_SYNC	PCM Synchronization control		O
29	NC5	Floating		I/O
30	NC6	Floating		Floating
31	GND4	Ground.		GND
32	NC7	Floating		I/O
33	GND5	Ground.		GND
34	BT_REG_ON	Used by PMU to power up or power down the		I

		internal regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.		
35	NC8	Floating		I/O
36	GND	Ground		GND
37	GPIO6	GPIO configuration pin		I/O
38	GPIO4	SECI_IN		I/O
39	GPIO2	GPIO configuration pin		I/O
40	GPIO5	SECI_OUT		I/O
41	UART_RTS_N	High-Speed UART RTS		O
42	UART_TXD	High-Speed UART Data Out		O
43	UART_RXD	High-Speed UART Data In		I
44	UART_CTS_N	High-Speed UART CTS		I
45	TP1	Floating		I/O
46	TP2	Floating		I/O
47	GPIO1_P7	GPIO configuration pin		I/O

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the VBAT and PA driver supply	-0.5	-	+5.0	V
V IO	DC supply voltage for digital I/O	-0.5	-	2.20	V
VDDIO RF	DC supply voltage for RF switch I/Os	-0.5	-	4.10	V
Tj	Maximum junction temperature	-	-	125	˚C
TBD	Maximum input power for RX input portsb	-	-	0	dBM

3.2 Recommended Operating Conditions

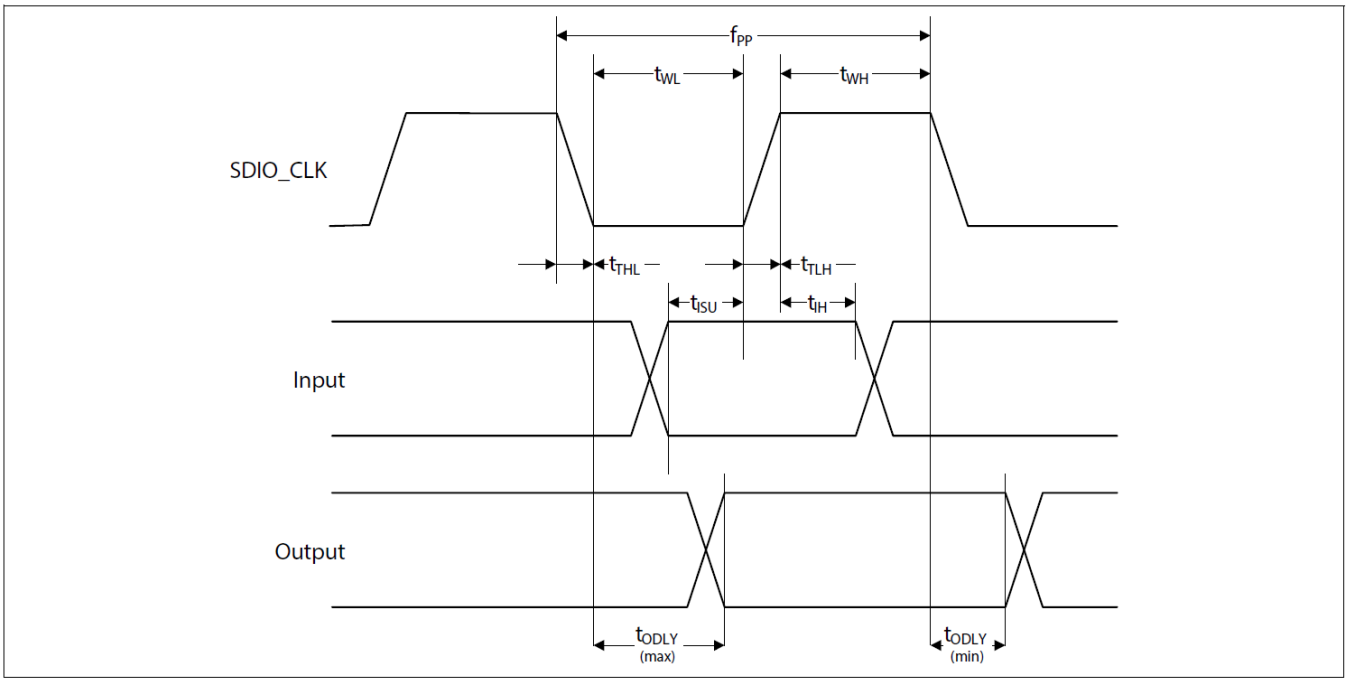
Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulator and FEM	3.2	3.6	4.4	V
VDDIO	DC supply voltage for digital I/O	1.62	1.8	1.98	V

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VIH	Input high voltage (VDDIO)	0.65 x VDDIO	-	-	V
VIL	Input low voltage (VDDIO)	-	-	0.35 × VDDIO	V
VOH	Output High Voltage @ 2mA	VDDIO – 0.45	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.45	V

3.4 Power up Timing Sequence

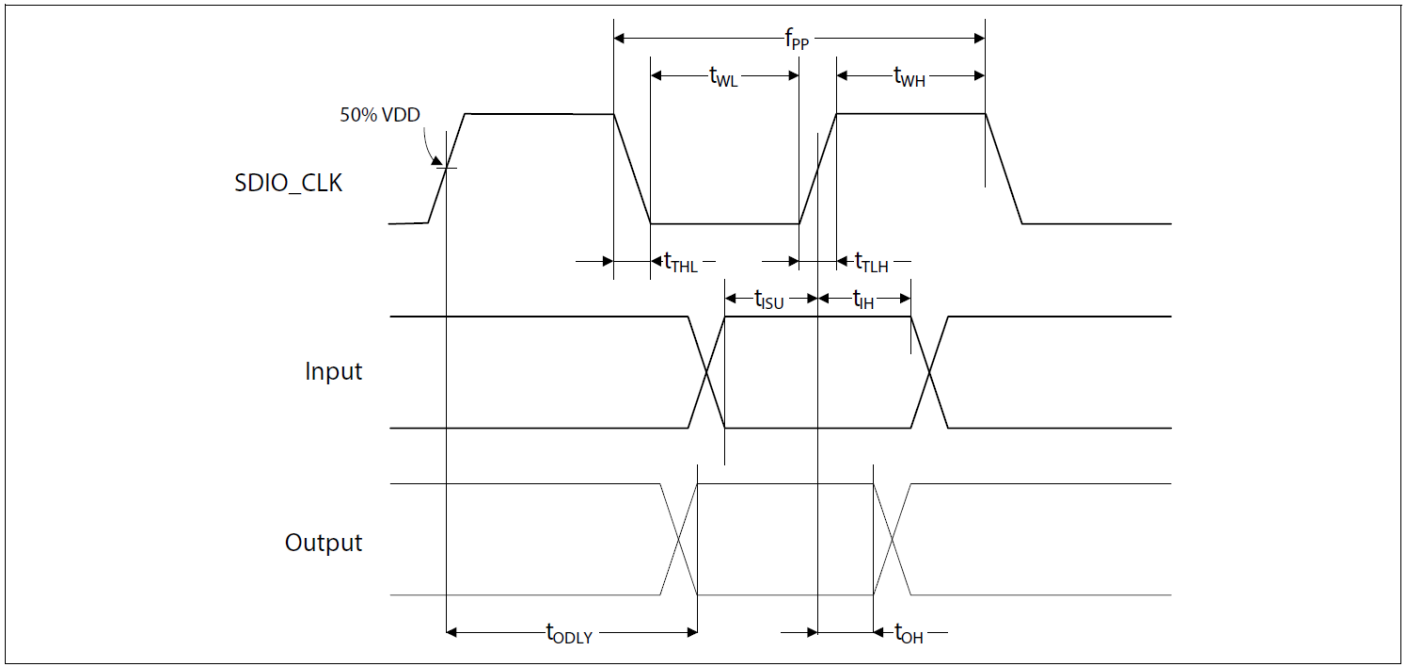
3.4.1 SDIO Host Interface Specification



SDIO Bus Timing (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL)					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

SDIO Bus Timing Parameters (Default Mode)



SDIO Bus Timing (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (refer- enced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (refer- enced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

SDIO Bus Timing a Parameters (High-Speed Mode)

3.4.2 UART Interface

The BT HCI UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 115200 bps to 4.0 Mbps.

The interface features an automatic baud rate detection capability that returns a baud rate selection. The baud rate may be changed using a vendor-specific UART HCI command.

The UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth UART HCI H4 specification. The default baud rate is 115.2 Kbaud.

The AW-AM497 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP).

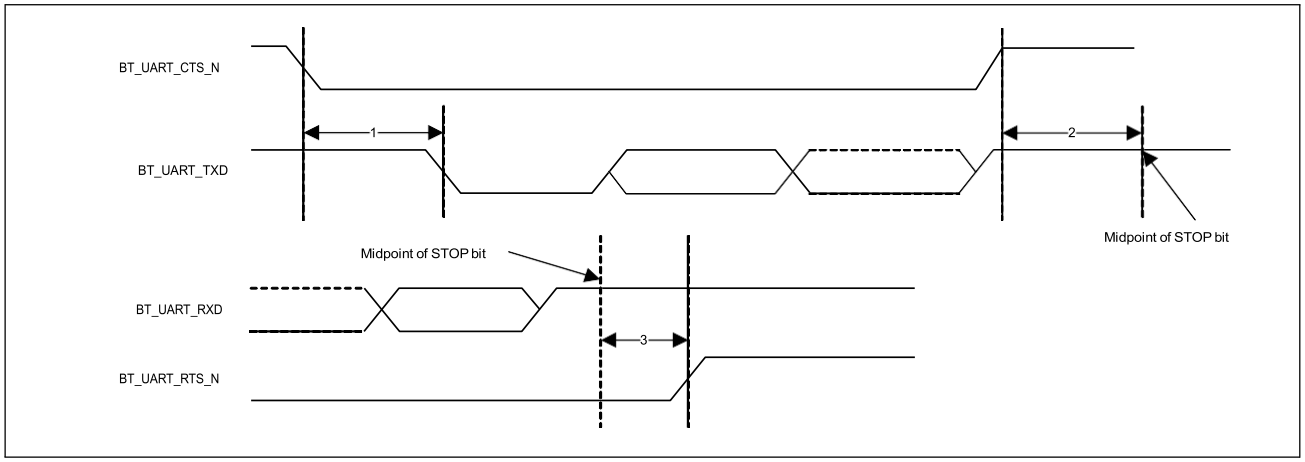
It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The AW-AM497 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

UART Interface Signals

Pin Number	Signal Name	Description	Type
42	BT_UART_TXD	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface	O
43	BT_UART_RXD	Bluetooth UART Series Input. Serial data input for the HCI UART Interface	I
41	BT_UART_RTS_N	Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface	I
44	BT_UART_CTS_N	Bluetooth UART Clear-to-Send. Active-low clear-to-send signal for the HCI UART interface.	O



UART Timing

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

UART Timing Specifications

3.4.3 Sequencing of Reset and Regulator Control Signals

The AW-AM497 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals

WL_REG_ON: Used by the PMU to power-up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal AW-AM497 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.

BT_REG_ON: Used by the PMU (OR-gated with WL REG ON) to power-up the internal AW-AM497 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note: The AW-AM497 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating Host SDIO, UART or SPI accesses.

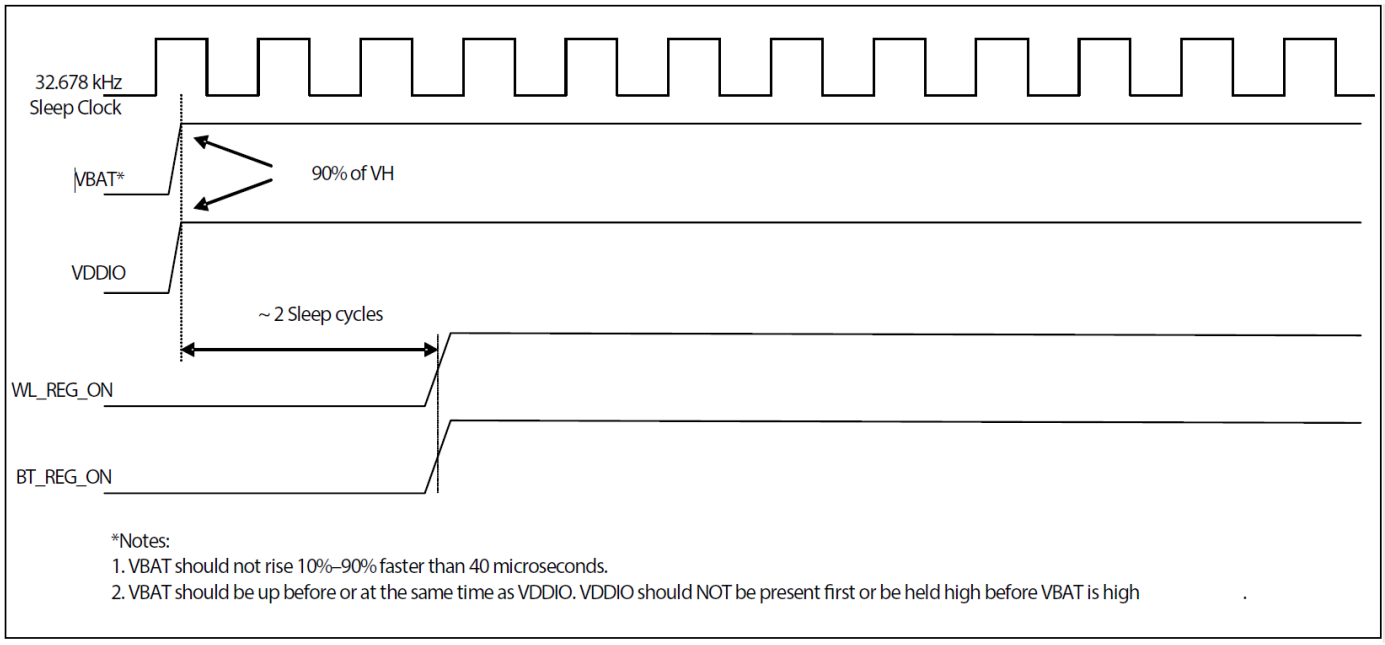
Note: VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Power-Up/Power-Down/Reset Circuits

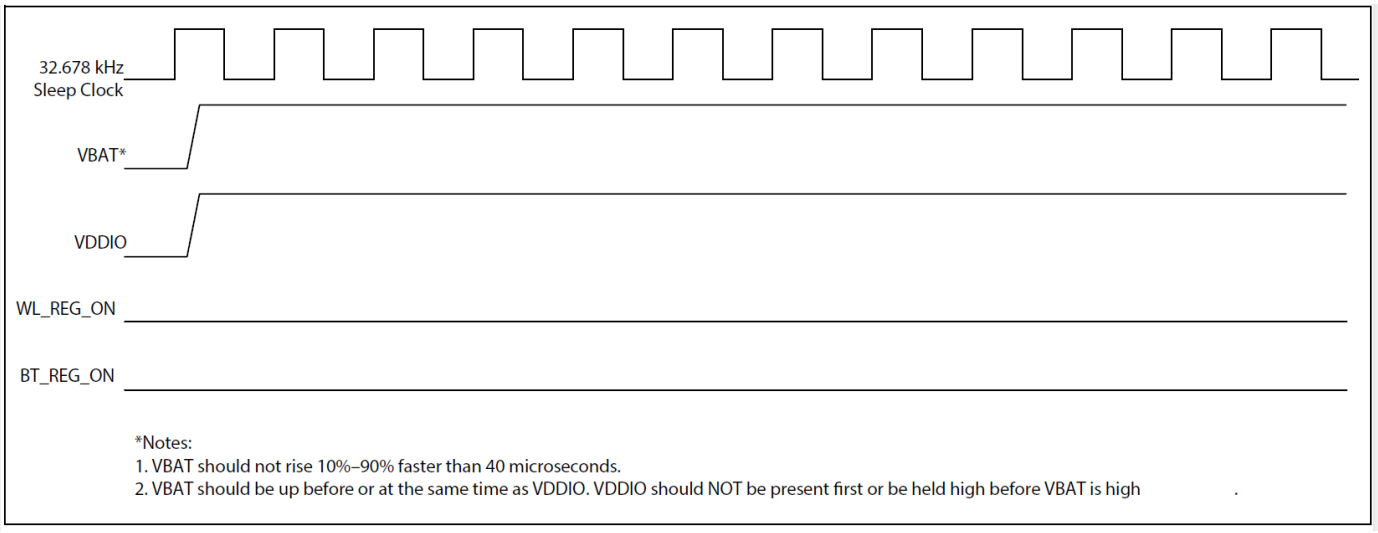
The AW-AM497 has two signals that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption.

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power-up the WLAN section. It is also OR-gated with the BT EG ON input to control the internal AW-AM497 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 50 kΩ pull-down resistor that is auto enabled and disabled when the input is low and high, respectively
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal AW-AM497 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 50 kΩ pull-down resistor that is auto enabled and disabled when the input is low and high, respectively.

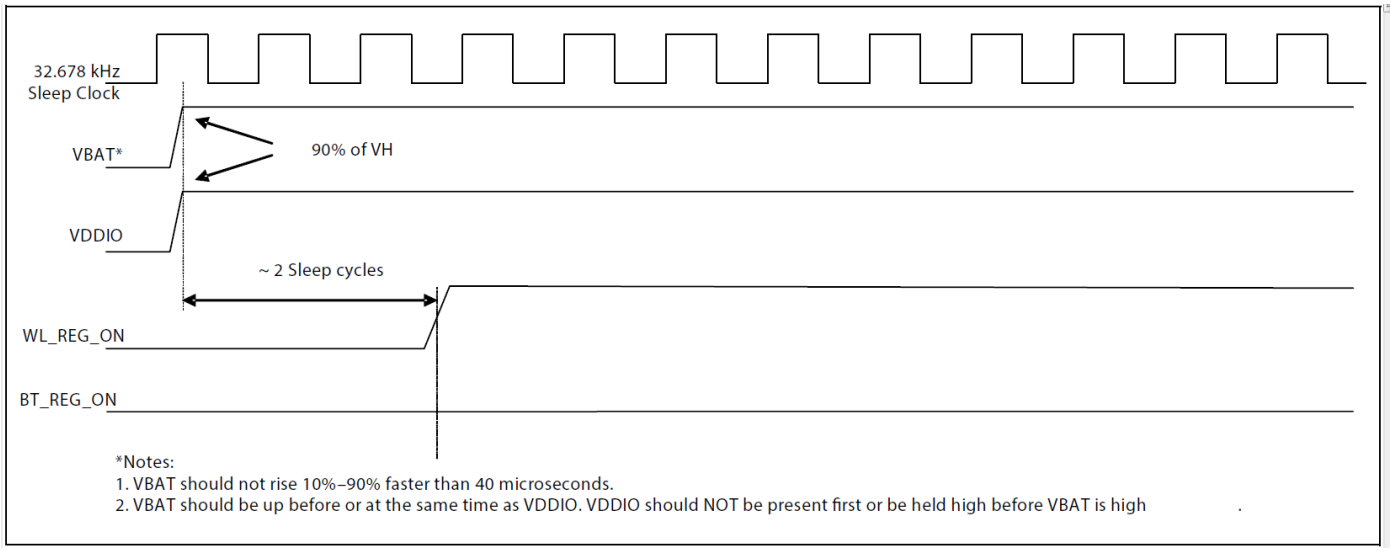
Power-Up/Power-Down/Reset Control Signals



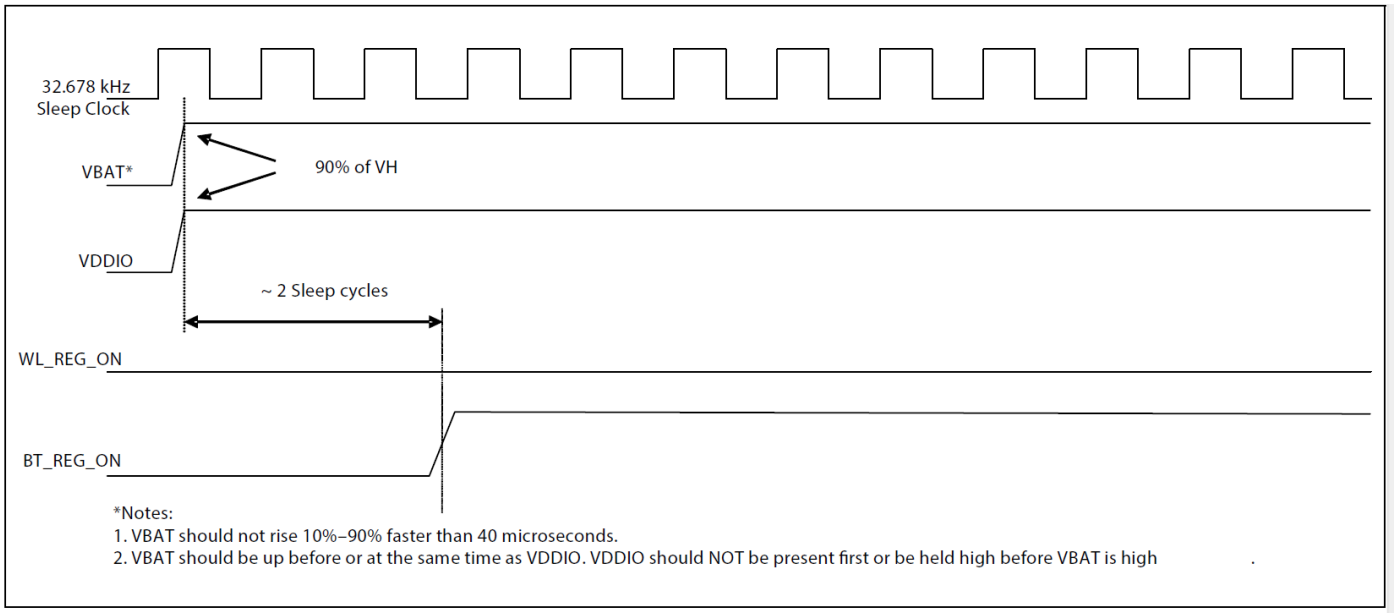
WLAN = ON, Bluetooth = ON



WLAN = OFF, Bluetooth = OFF



WLAN = ON, Bluetooth = OFF



WLAN = OFF, Bluetooth = ON

3.5 Power Consumption*

3.5.1 WLAN

No.	Item			VBAT=3.3V(mA)		
				Max.	Avg.	
1	WLAN OFF *(1)			1.9uA		
2	Sleep *(3)			3.0uA	2.9uA	
3	Power Save DTIM1 (2.4GHz) *(4) (6)			14.1mA	309uA	
4	Power Save DTIM3 (2.4GHz) *(5) (6)			23.1mA	233uA	
5	Power Save DTIM1 (5GHz) *(4) (6)			14.2mA	230uA	
6	Power Save DTIM3 (5GHz) *(5) (6)			15.5mA	127uA	
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit		
				Max.	Avg.	Duty (%)
2.4	11b@1Mbps	20	18	202	201	98
	11g@54Mbps	20	15	124	122	64
	11n@MCS7	20	15	119	118	67
5	11a@54Mbps	20	13	177	176	66
	11n@MCS7	20	13	173	172	68
	11ac@MCS8 NSS1	20	10	154	153	49
Band (GHz)	Mode	BW(MHz)		Receive		
				Max.	Avg.	
2.4	11b@1Mbps	20		21.1	19.8	
	11n@MCS7	20		20.8	20.1	
5	11a@54Mbps	20		23.2	22.3	
	11ac@MCS8 NSS1	20		24.1	23.1	

* The power consumption is based on Azurewave test environment, these data for reference only.

No.	Item			VDDIO=1.8 V	
				Max.	Avg.
1	WLAN OFF *(1)			0.29uA	
2	Sleep *(3)			105uA	105uA
3	Power Save DTIM1 (2.4GHz) *(4) (6)			376uA	111uA
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit	
				Max.	Avg.
2.4	11b@1Mbps	20	18	2.3mA	2.3mA
Band (GHz)	Mode	BW(MHz)		Receive	
				Max.	Avg.
2.4	11b@1Mbps	20		429uA	424uA

3.5.2 Bluetooth

No.	Mode	Packet Type	RF Power (dBm)	VBAT=3.3 V	
				Max.	Avg.
1	Sleep	n/a	n/a	3.8uA	2.9uA
2	Transmit *(1)	DH5	9.5	24mA	23mA
3	Receive *(1)	DH5	n/a	9.6mA	9.5mA
4	Transmit*(2)	LE	9.4	19.9mA	19.7mA
5	Receive	LE	n/a	10.4mA	10.4mA

* The power consumption is based on Azurewave test environment, these data for reference only.

3.6 Frequency Reference

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

External 32.768KHz Low-Power Oscillator

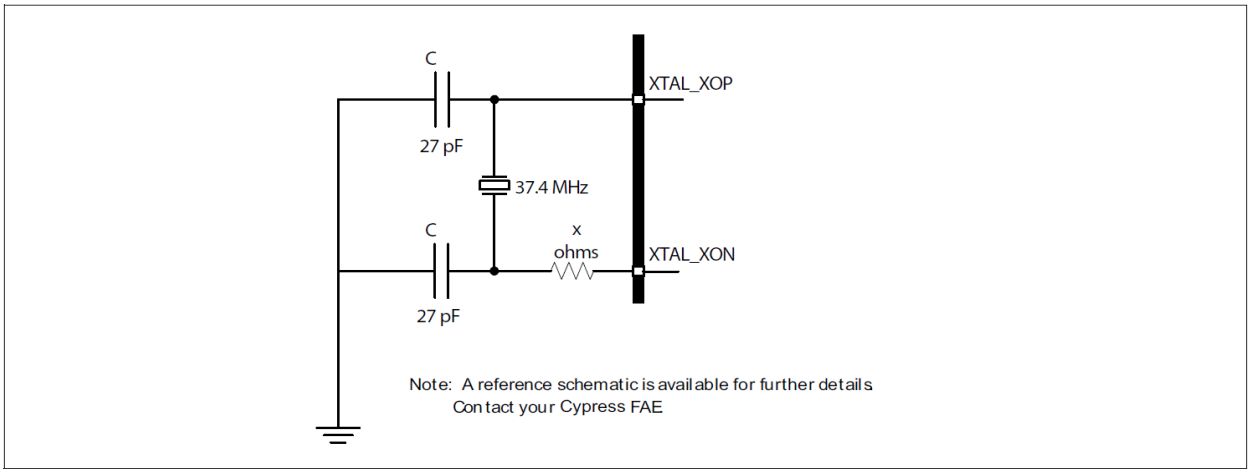
The AW-AM497 uses a secondary low frequency clock for low-power-mode timing. Either the internal low- precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake-up earlier to avoid missing beacons. Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in below.

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30–70	%
Input signal amplitude	500–1800	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance [a]	>100k	Ω

External 32.768 kHz Sleep Clock Specifications

Crystal Interface and Clock Generation

The AW-AM497 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in below. Consult the reference schematics for the latest configuration.



Recommended Oscillator Configuration

A fractional-N synthesizer in the AW-AM497 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

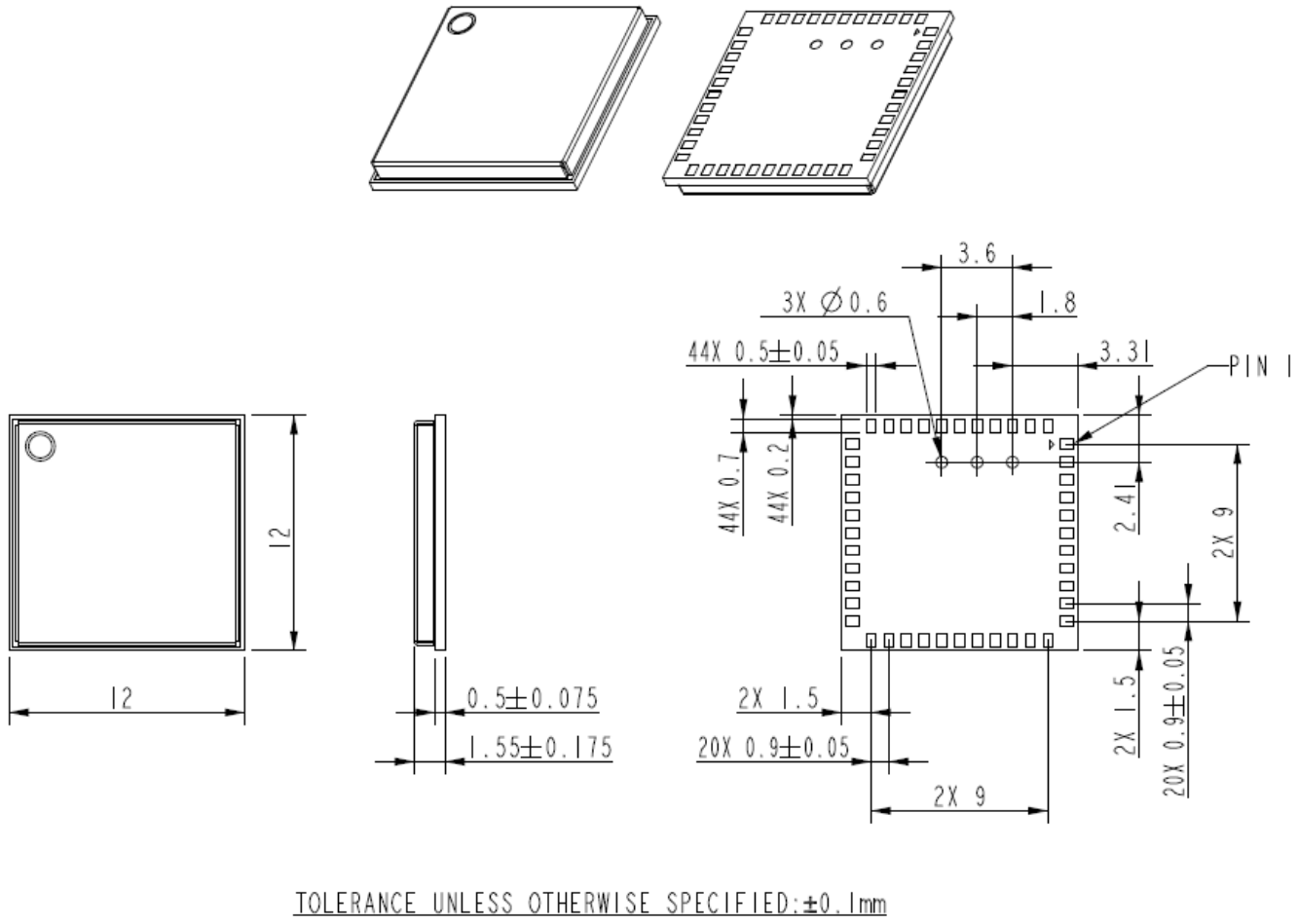
Parameter	Condition notes	Crystal[a]			External Frequency Reference [b, c]			
		Min	Typ	Max.	Min.	Typ.	Max.	Units
Frequency	2.4G and 5G bands	–	37.4	–	–	37.4	–	MHz
Frequency tolerance Without trimming over the lifetime of the equipment, including Temperature[d]	Without trimming	–20	–	20	–20	–	20	ppm
Crystal load capaci- tance	–	–	16	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	–	–	–	µW
Input impedance (XTAL_XOP)	Resistive	–	–	–	30k	100 k	–	Ω
	Capacitive	–	–	7.5	–	–	7.5	pF
XTAL_XOP Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
XTAL_XOP Input high level	DC-coupled digital signal	–	–	–	0.9	–	1.1	V
XTAL_XOP input voltage	IEEE 802.11a/b/g operation only	–	–	–	400	–	1100	mVp-p
XTAL_XOP input voltage	IEEE 802.11a/b/g operation only	–	–	–	1	–	–	Vp-p
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise[e] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz
	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–142	dBc/Hz

Phase Noise[e] (IEEE 802.11n,5 GHz)	37.4 MHz clock at 100 kHz offset–	–	–	–	–	–	–149	dBc/Hz

The recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal interface are listed in table below.

4. Mechanical Information

4.1 Mechanical Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

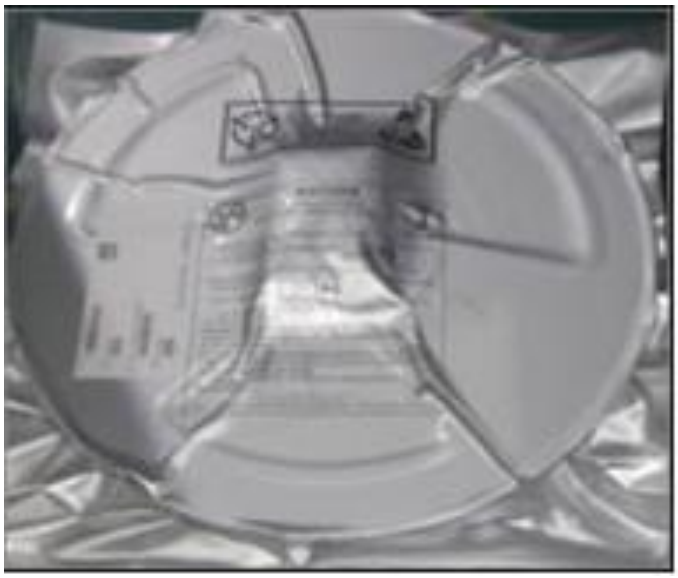
Unit:mm

5. Packaging Information

1. One reel = 1,500pcs 12*12 LGA module.
   (一卷數量為 1500pcs.)

2. One production label is pasted on the reel.
   One desiccant & one humidity indicator card are put on the reel.
   (卷軸貼上一張生產標籤，同時放上一包防潮包及濕度指示卡.)

3.One reel is put into the anti-static moisture barrier bag with one production label on the bag.
(卷軸放進入防靜電鋁袋，再貼上生產標籤.)



4. The anti-static reel is put into the pink bubble wrap.
(防靜電鋁箔袋放進氣泡袋.)
Then put into the inner box with one production label pasted on the box.
(氣泡袋放進內箱中，再貼上一張生產標籤.)

5. One outer box contained 5 inner boxes.
(一個外箱可放五個內箱盒.)

6. Sealing the carton with Azurewave logo tape.
(使用海華 Logo 膠帶將外箱進行工字型封箱)

7. One carton label and one box label are pasted on the carton.
If one carton is not full, one balance label will be pasted on the carton
(外箱上貼附出貨標籤和箱號標籤；如不滿箱，需貼附尾數標籤)