AW-CM276NF

IEEE 802.11 2X2 MU-MIMO ac/a/b/g/n Wireless LAN + Bluetooth 5.0 NGFF Module

Datasheet

Version 1.4

Document release	Date	Modification	Initials	Approved
Version0.1	2016/03/02	Initial version	Renton Tao	Daniel Lee
Version0.2	2016/06/06	1. Update Block diagram 2. Update pin definition 3. Update mechanical drawing	Renton Tao	Daniel Lee
Version0.3	2016/09/12	1. Update pin map 2. Add pin out drawing 3. Remove G17 and G18	Renton Tao	Daniel Lee
Version0.4	2016/11/02	1. Update pin out drawing 2. Add RF spec	Renton Tao	Daniel Lee
Version0.5	2016/12/6	1. Update Specifications Table 2. Configuration pins 3. shipping information	Renton Tao	Daniel Lee
Version0.6	2017/1/13	1. Update BDR power 2. Update pin definitions.	Renton Tao	Daniel Lee
Version0.7	2017/2/13	Update ESD test conditions	Renton Tao	Daniel Lee
Version0.8	2017/3/2	Update Operating conditions	Renton Tao	Daniel Lee
Version0.9	2017/6/16	1. Update key feature 2. Adding RF connector information	Renton Tao	Daniel Lee
Version1.0	2018/02/21	Update BT 4.2 to BT5.0	Renton Tao	Daniel Lee
Version1.1	2018/06/21	Update output power table	Renton Tao	NC Chen
Version1.2	2018/08/2	Revise output power table	Renton Tao	NC Chen
Version1.3	2018/08/7	Update 1-3. Key feature 1-4. Specifications Table	Renton Tao	NC Chen

Version1.4	**2019/07/10**	**Update** **4. Pin Definition**	**Renton Tao**	**NC Chen**

1. General Description

1-1. Product Overview and Functional Description

AzureWave Technologies, Inc. introduces the IEEE 802.11ac/a/b/g/n 2X2 MU-MIMO WLAN & Bluetooth NGFF module --- **AW-CM276NF**. The module is targeted to mobile devices including **Notebook, TV, Tablet and Gaming Device** which need small package module, low power consumption, multiple interfaces and OS support. By using AW-CM276NF, the customers can easily enable the Wi-Fi, and BT embedded applications with the benefits of **high design flexibility, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11ac/a/b/g/n standard supporting 802.11ac Wave 2, the AW-CM276NF uses Direct Sequence Spread Spectrum (**DSSS**), Orthogonal Frequency Division Multiplexing (**OFDM**), **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CM276NF. In addition to the support of **WPA/WPA2** and **WEP** 64-bit and 128-bit encryption, the AW-CM276NF also supports the **IEEE 802.11i** security standard through the implementation of **Advanced Encryption Standard** (**AES)/Counter Mode CBC-MAC Protocol (CCMP),** Wired Equivalent Privacy (**WEP)** with Temporal Key Integrity Protocol (**TKIP)**, Advanced Encryption Standard (**AES**)/Cipher-Based Message Authentication Code (**CMAC**), and WLAN Authentication and Privacy Infrastructure (**WAPI**) security mechanisms.

For the video, voice and multimedia applications the AW-CM276NF support **802.11e Quality of Service** (**QoS).** The device also supports **802.11h Dynamic Frequency Selection (DFS)** for detecting radar pulses when operating in the 5GHz range.

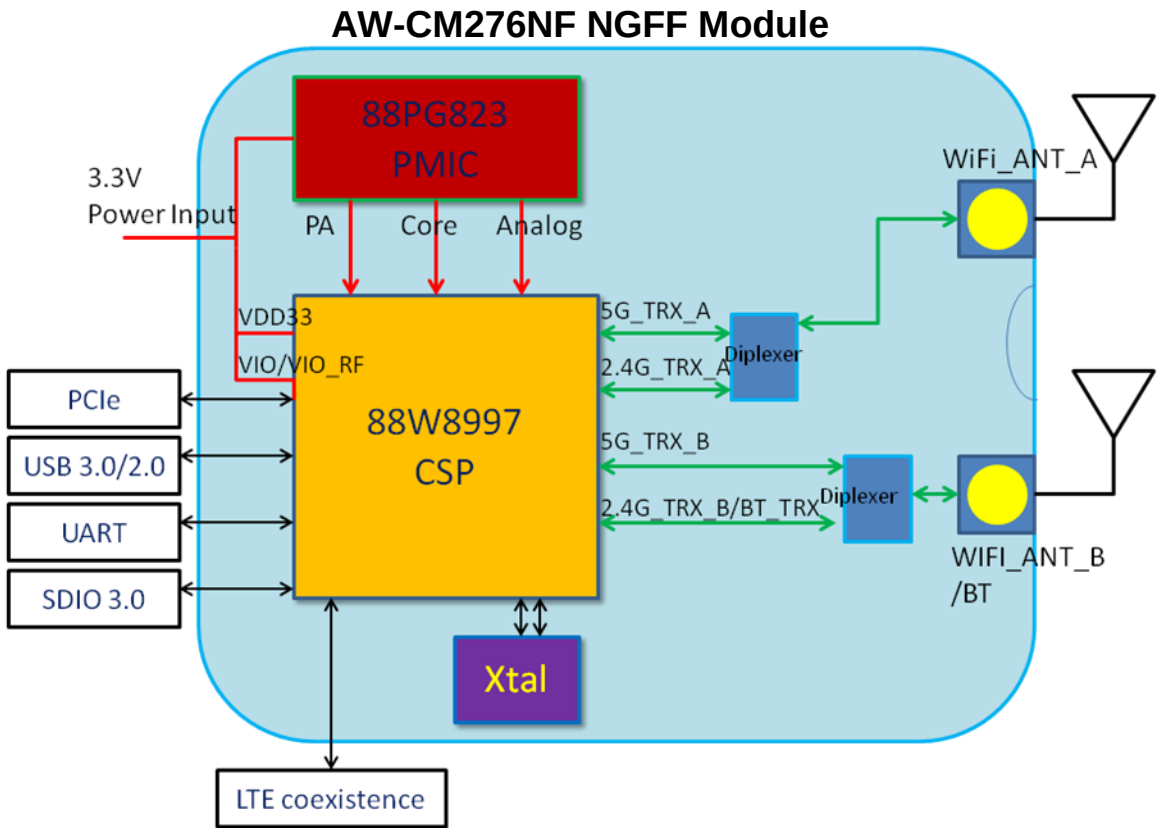
For Bluetooth operation, AW-CM276NF is **Bluetooth 5.0 (supports Low Energy).**

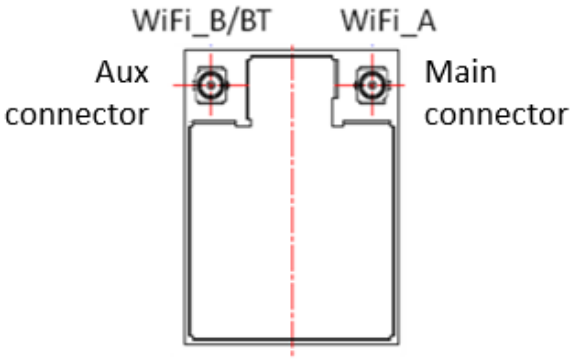
AW-CM276NF supports **PCIE, USB 3.0/2.0,** and high speed **UART interfaces** for WLAN and Bluetooth to the host processor.

AW-CM276NF is suitable for multiple mobile processors for different applications with the support **cellular phone co-existence**.

AW-CM276NF module adopts Marvell's latest highly-integrated dual-band WLAN & Bluetooth SoC--- **88W8997**. All the other components are implemented by all means to reach the mechanical specification required.

1-2. Block Diagram





Module antenna configuration

1-3. Key feature:

- PCIe M.2 TYPE 1216: 16mm(L) x 12mm(W) x 1.85 mm(H)(Max)
- SDIO 3.0, PCIe, USB 3.0/2.0 interfaces support for WLAN
- USB 3.0/2.0, UART interfaces support for Bluetooth
- High speed UART,PCM interfaces
- Bluetooth 5.0 complaint with Bluetooth 2.1 + Enhanced Data Rate (EDR)
- Audio Codec interface support
- Sub-meter accuracy WiFi indoor locationing(802.11mc)
- Multiple power saving modes for low power consumption
- IEEE 802.11i for advanced security
- Quality of Service (QoS) support for multimedia applications
- Support China WAPI
- Lead-free design
- Support optional VIO level(default 1.8V)

1-4. Specifications Table

<table>
<tr><th>Model Name</th><th>AW-CM276NF</th></tr>
<tr><th>Product Description</th><th>2x2 MU-MIMO Wireless LAN + Bluetooth Combo Module</th></tr>
<tr><td>WLAN Standard</td><td>IEEE 802.11 ac/a/b/g/n, Wi-Fi compliant</td></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 5.0 complaint with Bluetooth 2.1+Enhanced Data Rate (EDR)</td></tr>
<tr><td>Host Interface</td><td>PCIe/SDIO/USB for WLAN, USB/UART for Bluetooth</td></tr>
<tr><td>Major Chipset</td><td>Marvell 88W8997</td></tr>
<tr><td>Dimension</td><td>12mm(W) x 16mm(L) x 1.85mm(H)</td></tr>
<tr><td>Weight</td><td>0.0005 kg</td></tr>
<tr><td>Package</td><td>LGA</td></tr>
<tr><th colspan="2">Operating Conditions</th></tr>
<tr><td>Voltage</td><td>3.3V+- 10%</td></tr>
<tr><td>Temperature</td><td>Operating: -30~ 85ºC ; Storage: -40~ 125ºC</td></tr>
<tr><th colspan="2">Electrical Specifications</th></tr>
<tr><td>Frequency Range</td><td>2.4 GHz ISM radio band / 5 GHz Unlicensed National Information Infrastructure (U-NII) band</td></tr>
<tr><td>Number of Channels</td><td>802.11ac(VHT20): 36,40,44,48,52,56,60,64,100,104,108,112,116,120,
124,128,132,136,140,149,153,157,161,165
802.11ac(VHT40): 38,46,54,62,102,110,118,126,134,151,159
802.11ac(VHT80): 42,58,106,122,138,155
802.11a: USA–36,40,44,48,52,56,60,64,100,104,108,112,116,120,
124,128,132,136,140,149,153,157,161,165
802.11b: USA, Canada and Taiwan – 1~11
Most European Countries – 1~13
802.11g: USA, Canada and Taiwan – 1~11
Most European Countries – 1~13
802.11n(HT20): Channel 1~13(2412~2472)
802.11n(HT40): Channel 1~7(2422~2452)</td></tr>
<tr><td>Modulation</td><td>DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM and 256-QAM for WLAN
GFSK (1Mbps), Π/4 DQPSK (2Mbps) and 8DPSK (3Mbps) for Bluetooth</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><th>WLAN 2.4GHz band</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>11b 11Mbps@EVM≦35%</td><td>15.5</td><td>17</td><td>18.5</td></tr>
<tr><td>11g 54Mbps@EVM≦-27dB</td><td>14.5</td><td>16</td><td>17.5</td></tr>
<tr><td>11n HT20 MCS7@EVM≦-28dB</td><td>14.5</td><td>16</td><td>17.5</td></tr>
<tr><td>11n HT40 MCS7@EVM≦-28dB</td><td>12.5</td><td>14</td><td>15.5</td></tr>
</table>
Unit:dBm
<table>
<tr><th>WLAN 5GHz band</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>11a 54Mbps@EVM≦-27dB</td><td>11</td><td>13</td><td>15</td></tr>
<tr><td>11n HT20 MCS7@EVM≦-28dB</td><td>11</td><td>13</td><td>15</td></tr>
<tr><td>11n HT40 MCS7@EVM≦-28dB</td><td>10</td><td>12</td><td>14</td></tr>
<tr><td>11ac VHT20 MCS8@EVM≦-30dB</td><td>11</td><td>13</td><td>15</td></tr>
<tr><td>11ac VHT40 MCS9@EVM≦-32dB</td><td>10</td><td>12</td><td>14</td></tr>
<tr><td>11ac VHT80 MCS9@EVM≦-32dB</td><td>8</td><td>10</td><td>12</td></tr>
</table>
Unit:dBm
<table>
<tr><th>BT</th><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>BDR/BLE</td><td>0</td><td>2</td><td>4</td></tr>
</table>
</td></tr>
</table>

Antenna Connector	**Main Connector: WLAN Aux Connector: WLAN + BT**
Receive Sensitivity	**Minimum sensitivity(typ):** **WLAN 2.4GHz band:** **11b 11M: -88dBm** **11g 54M: -75dBm** **11n MCS7 BW20: -72dBm** **11n MCS7 BW40: -69dBm** **WLAN 5GHz band:** **11a 54M: -72dBm** **11n BW20 MCS7: -69dBm** **11n BW40 MCS7: -68dBm** **11ac BW20 MCS8: -65dBm** **11ac BW40 MCS9: -63dBm** **11ac BW80 MCS9: --60dBm** **Bluetooth:** **BDR: -83dBm**
Medium Access Protocol	**CSMA/CA with ACK**
Data Rates	**WLAN** **802.11b: 1, 2, 5.5, 11Mbps** **802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps** **802.11n: up to 150Mbps-single** **802.11n: up to 300Mbps-2x2 MIMO** **802.11ac:up to 192.6Mbps (20MHz channel)** **802.11ac:up to 400Mbps (40MHz channel)** **802.11ac:up to 866.7Mbps (80MHz channel)** **Bluetooth** **Bluetooth 5.0** **Bluetooth 2.1+EDR data rates of 1,2, and 3Mbps**
Power Consumption	**Please refer to test report.**
Operating Range	**Open Space: ~300m ; Indoor: ~100m for WLAN** **Minimum 10 m indoor for Bluetooth** **The transmission speed may vary according to the environment)**
Security	◆ **WAPI** ◆ **WEP 64-bit and 128-bit encryption with H/W TKIP processing** ◆ **WPA/WPA2 (Wi-Fi Protected Access)** ◆ **AES-CCMP hardware implementation as part of 802.11i security standard**
ESD test condition	**HBM: +-2KV** **CDM: +-500V**
Operating System Compatibility	**Linux(Android), More information please contact Azurewave FAE.**
Co-Existence	**Please refer to test report.**

***WiFi /BT power & sensitivity measure @ module out**

2. Electrical Characteristic

2-1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Units
Pin73/ VIO	Host I/O power supply	-- -- --	-- -- --	1.8 2.5 3.3	2.2 3.0 4.0	V
Pin44/ VIO_SD	SDIO power supply	-- --	-- --	1.8 3.3	2.2 4.0	V
Pin4,5,72/ 3.3V	3.3V VBAT input	--	--	3.3	3.63	V
$T_{storage}$	Storage Temperature		-40		125	℃

2-2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Pin73/ VIO	1.8V/2.5V/3.3V digital I/O power supply	-- -- --	1.62 2.25 2.97	1.8 2.5 3.3	1.98 2.75 3.63	V
Pin44/ VIO_SD	1.8V/3.3V digital I/O SDIO power supply	-- --	1.62 2.97	1.8 3.3	1.98 3.63	V
Pin4,5,72/ 3.3V	3.3V VBAT input	--	2.97	3.3	3.63	V
T_A	Ambient operating temperature	--	-30		85	℃

2-3. Clock Specifications

2-3.1 External Sleep Clock Timing

External Sleep Clock is necessary for two reasons:

1. Auto frequency Detection.

   This is where the internal logic will bin the Ref clock source to figure out what is the reference clock frequency is. This is done so no strapping is needed for telling 88W8997 what the ref clock input is.

2. Allow low current modes for BT to enter sleep modes such as sniff modes.

   The AW-CM276NF external sleep clock pin is powered from the 3.3V voltage supply.

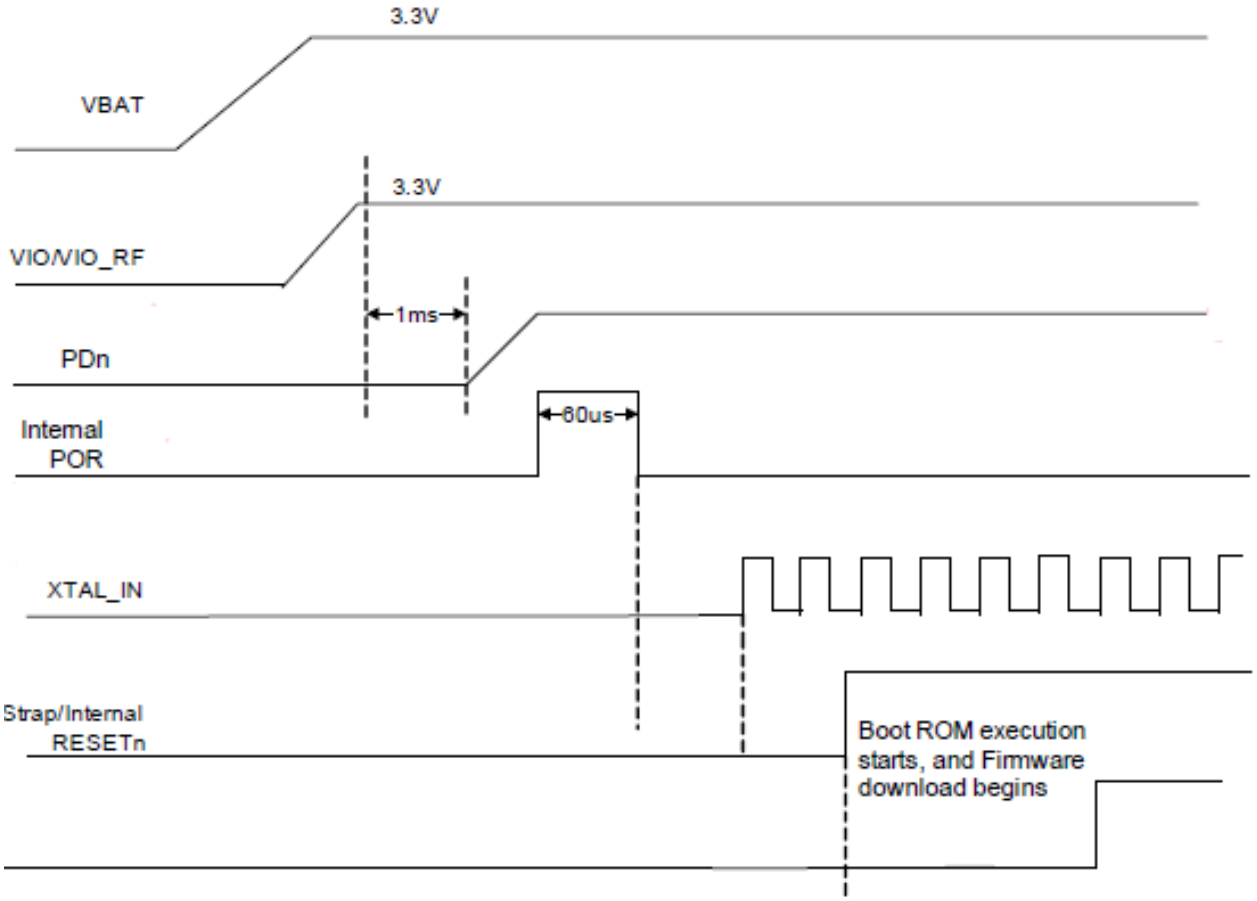
Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock Frequency Range/accuracy +-250ppm(initial, aging, temperature)		32.768		KHz

2-4. Reset Configuration

The AW-CM276NF is reset to its default operating state under the following conditions:

- Power-on reset (POR)
- Software/Firmware reset
- External pin for power down (PDn)

2-5. Power up Timing Sequence



3. Host Interfaces

3-1. SDIO Interface

The AW-CM276NF supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless module device.

The AW-CM276NF acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

The SDIO device interface main features include:

Supports SDIO 3.0 Standard

On-chip memory used for CIS

Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes

Special interrupt register for information exchange

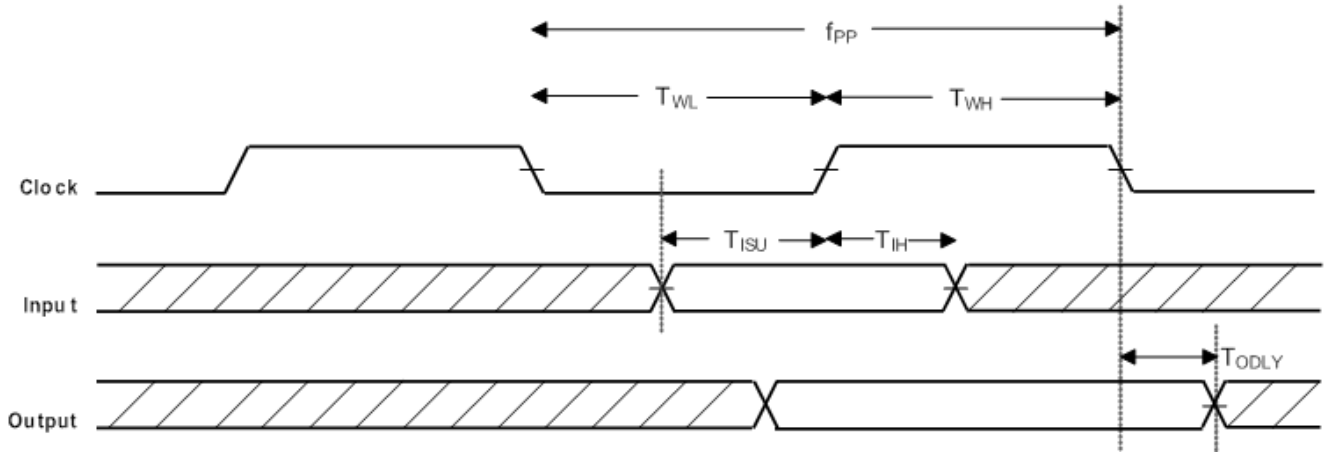
Allows card to interrupt host

3-1-1. SDIO Interface Signal Description

Pin Name	Signal Name	Type	Description
SD_CLK	CLK	I/O	SDIO 1-bit mode: Clock SDIO SPI mode: Clock
SD_CMD	CMD	I/O	SDIO 1-bit mode: Command line SDIO SPI mode: Data input
SD_DAT[3]	DAT3	I/O	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used SDIO SPI mode: Chip select (active low)
SD_DAT[2]	DAT2	I/O	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPII mode: Reserved
SD_DAT[1]	DAT1	I/O	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt SDIO SPI mode: Interrupt
SD_DAT[0]	DAT0	I/O	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line SDIO SPI mode: Data output

3-1-2. Default Speed, High Speed Modes (3.3V)

SDIO Protocol Timing Diagram – Default Speed Mode (3.3V)



SDIO Protocol Timing Diagram – HighSpeed Mode (3.3V)

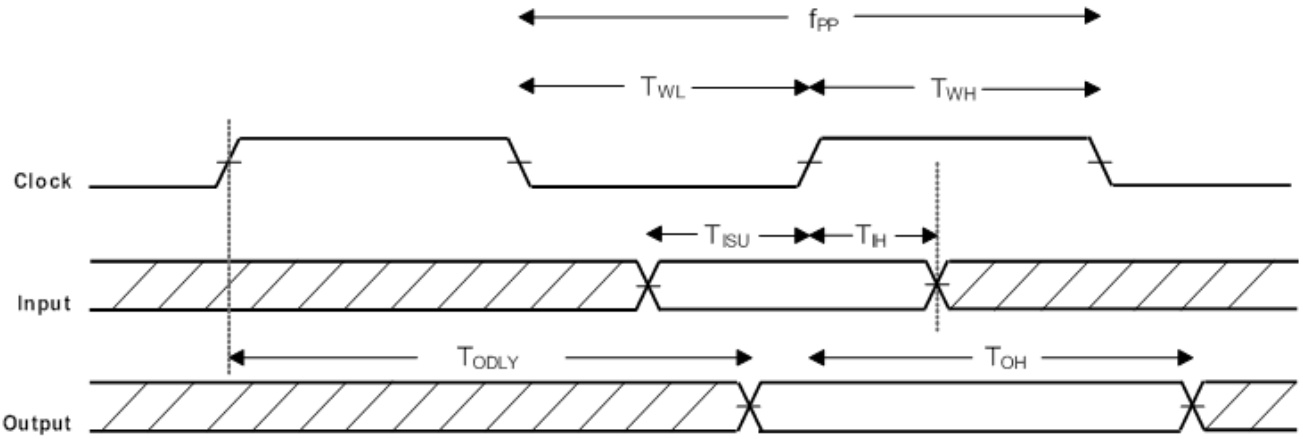


Table shows SDIO Timing Data—Default Speed, High Speed Modes (3.3V)

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency	Default Speed	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WL}	Clock Low Time	Default Speed	10	--	--	ns
		High Speed	7	--	--	ns
T_{WH}	Clock High Time	Default Speed	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Default Speed	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Default Speed	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time CL ≤ 40 pF (1 card)	Default Speed	--	--	14	ns
		High Speed	---	-1	4	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

3-1-3. SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

SDIO Protocol Timing Diagram – SDR12,SDR25,SDR50 Modes (up to 100MHz) (1.8V)

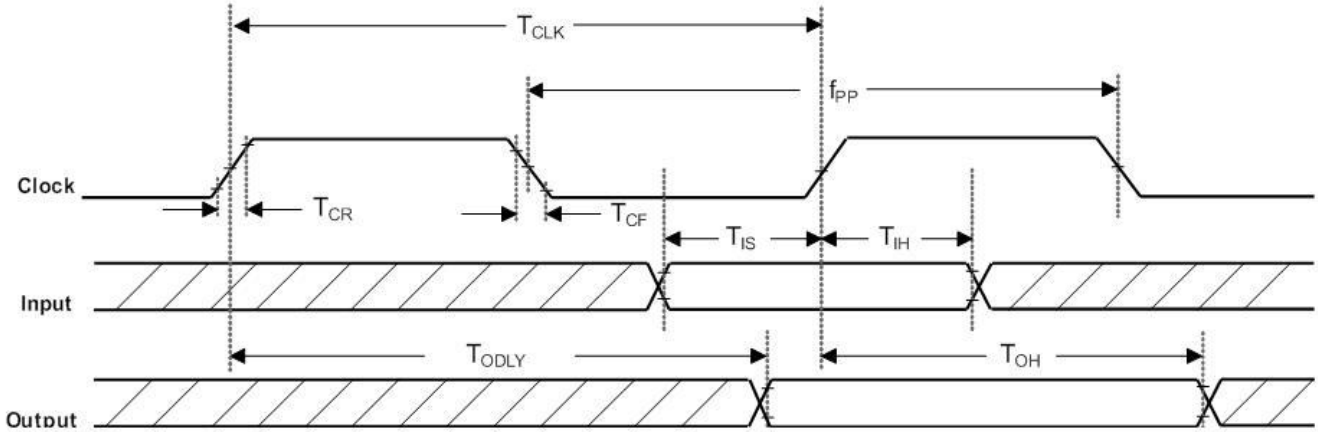


Table shows SDIO Timing Data—SDR12,SDR25,SDR50 Modes (up to 100MHz) (1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR12/25/50	25	--	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	--	--	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	--	--	ns
T_{CLK}	Clock time	SDR12/25/50	10	--	40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	--	--	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time $C_L \leq 30$ pF	SDR12/25/50	--	--	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	--	--	ns

3-1-4. SDR104 Modes (208MHz) (1.8V)

SDIO Protocol Timing Diagram –SDR104 Mode (208MHz)

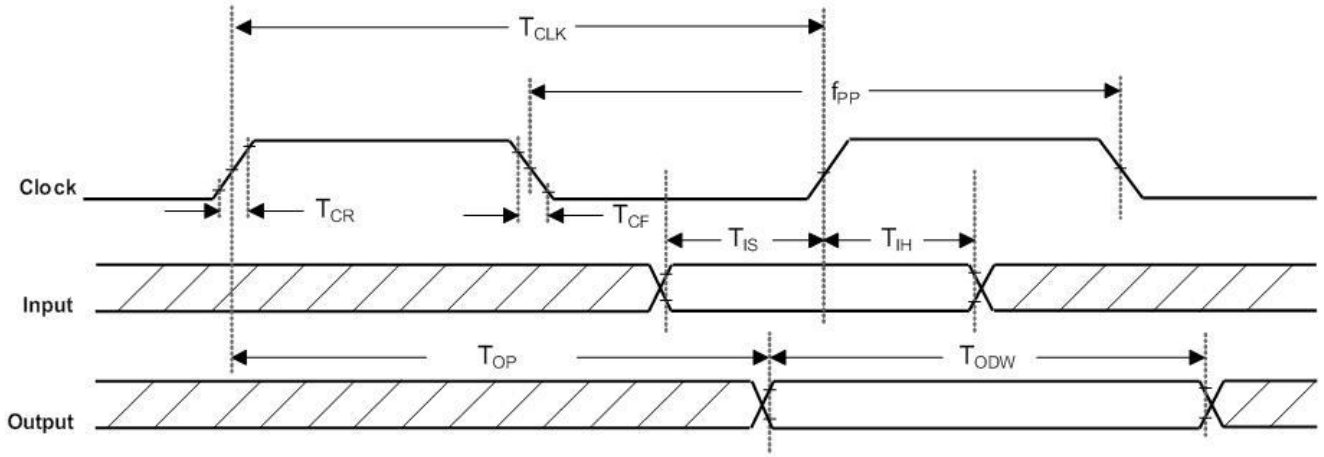


Table shows SDIO Timing Data—SDR104 Mode (208MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR104	0	--	208	MHz
T_{IS}	Input setup time	SDR104	1.4	--	--	ns
T_{IH}	Input hold time	SDR104	0.8	--	--	ns
T_{CLK}	Clock time	SDR104	4.8	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	--	--	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	--	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	--	--	ns

3-1. PCI Express Interface

3-1-1 Differential Tx Output Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps ±300 PPM. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
V_{Tx_DIFFpp}	Differential peak-to-peak output voltage $V_{Tx\_DIFFpp} = 2*\|V_{TX-D+} - V_{TX-D-}\|$	0.800	--	1.2	V
$V_{Tx\_DE\_RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	db
T_{Rx_EYE}	Minimum Tx eye width	0.75	--	--	UI
$T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$	Maximum time between jitter median and maximum deviation from median	--	--	0.125	UI
T_{Tx_RISE}, T_{Tx_FALL}	D+/D- Tx output rise/fall time	0.125	--	--	UI
$V_{Tx\_CM\_DC\_ACTIVE\_IDLE\_DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0-	-	100	mV
$V_{Tx\_CM\_DC\_LINE\_DELTA}$	Absolute delta of DC common mode voltage between D+ and D-	0-	-	25	mV
$V_{Tx\_IDLE\_DIFFp}$	Electrical idle differential peak output voltage	0	--	20	mV
$V_{Tx\_RCV\_DETECT}$	Voltage change allowed during receiver detection	--	--	600	mV
$V_{Tx\_DC\_CM}$	Tx DC common mode voltage	--	--	3.6	V
I_{Tx_SHORT}	Tx short circuit current limit	--	--	90	mA
$T_{Tx\_IDLE\_MIN}$	Minimum time spent in electrical idle	50	--	--	UI
$T_{Tx\_IDLE\_SET\_TO\_IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	--	--	20	UI
$T_{Tx\_IDLE\_TO\_DIFF\_DATA}$	Maximum time to transition to valid Tx specifications after leaving an electrical idle condition	--	--	20	UI
RL_{Tx_DIFF}	Differential return loss	10	--	--	dB
RL_{Tx_CM}	Common mode return loss	6	--	--	dB
C_{Tx}	AC coupling capacitor	75	--	200	nF
$T_{Crosstalk}$	Crosstalk random timeout	0	--	1	ms

3-1-2 Differential Rx Output Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
V_{Rx_DIFFpp}	Differential peak-to-peak voltage $V_{Rx\_DIFFpp} = 2*\|V_{RX-D+} - V_{RX-D-}\|$	0.175	--	1.2	V
T_{Rx_EYE}	Minimum receiver eye width	0.4	--	--	UI
$T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$	Maximum time between jitter median and maximum deviation from median	--	--	0.3	UI
$V_{Rx\_CM\_ACp}$	AC peak common mode input voltage	--	--	150	mV
RL_{Rx_DIFF}	Differential return loss	10	--	--	dB
RL_{Rx_CM}	Common mode return loss	6	--	--	dB
$Z_{Rx\_DIFF\_DC}$	DC differential input impedance	80	100	120	Ω
Z_{Rx_DC}	DC input impedance	40	50	60	Ω
$Z_{Rx\_HIGH\_IMP\_DC\_POS}$	Powered down DC input impedance positive	50	--	--	k
$Z_{Rx\_HIGH\_IMP\_DC\_NEG}$	Powered down DC input impedance negative	1	--	--	kΩ
$V_{Rx\_IDLE\_DET\_DIFFpp}$	Electrical idle detect threshold	65	--	175	mV
$T_{Rx\_IDLE\_DET\_DIFF\_ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	--	--	10	ms
L_{Rx_SKEW}	Total skew	---	-2	0	ns

3-2. USB Interface

The USB device interface is compliant with the Universal Serial Bus Specification, Revision 2.0, April 27, 2000. A USB host uses the USB cable bus and the USB 2.0 device interface to communicate with the chip.

The main features of the USB device interface include:

High/full speed operation (480/12 Mbps)

Suspend/host resume/device resume (remote wake-up)

Built-in DMA engine that reduces interrupt loads on the embedded processor and reduces the system bus bandwidth requirement for serving the USB device operation

The USB 2.0 device interface is designed with 3.3V signal level pads.

3-2-1. USB 2.0 Device Interface Description

Table shows the signal mapping between the AW-CM276NF and the USB Specification, Revision 2.0.

Pin Name	USB 2.0 Specification Pin Name	Description
Pin72/ 3V3_USB	VBUS	USB Bus Power Supply On-board regulator regulates voltage from VBUS level to voltage levels used by USB PHY.
	GND	USB Bus Ground Common ground on SoC device.
Pin70/ USB_DP	D+	USB Bus Data Positive. One of the differential data pair.
Pin69/ USB_DN	D-	USB Bus Data Negative. One of the differential data pair.

3-2-2. USB 2.0 Device Functional Description

The device controller uses internal Scatter/Gather DMA engine to transfer the transmit packet from internal SRAM to USB and the receive packet from USB to internal SRAM. The Device IN Endpoint DMA (DIEPDMAn) and Device OUT Endpoint DMA (DOEPDMAn) registers are used by the DMA engine to access the base descriptor. The application is interrupted after the programmed transfer size extracted from the descriptors is transmitted or received. By using registers, interrupts, and special data structures, the device controller can communicate with the device controller driver (application/software) about bus states, host request, and data transfer status. The device controller driver also has all of the routines to respond to the device framework commands issued by a USB host, so it controls the attachment, configuration, operation, and detachment of the device.

3-3. High-Speed UART Interface

The AW-CM276NF supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data. Table shows the rates supported.

The UART interface features include:

FIFO mode permanently selected for transmit and receive operations

Two pins for transmit and receive operations

Two flow control pins

Interrupt triggers for low-power, high throughput operation

The UART interface operation includes:

Upload boot code to the internal CPU (for debug purposes)

Support diagnostic tests

Support data input/output operations for peripheral devices connected through a standard UART interface

UART Baud Rates Supported

Baud Rate				
1200	38400	460800	1500000	3000000
2400	57600	500000	1843200	3250000
4800	76800	921600	2000000	3692300
9600	115200	1000000	2100000	4000000
19200	230400	1382400	2764800	--

3-3-1. UART Interface Signal Description

Table shows the standard UART signal names on the device.

Signal Name	16550 Standard Pin Name	Description
Data Bus		
UART_SIN	SIN	Serial data input from modem, data set, or peripheral device
UART_SOUT	SOUT	Serial data output from modem, data set, or peripheral device
Modem Control		
UART_RTSN	RTS	Request To Send output to modem, data set, or peripheral device (active low)
UART_CTSN	CTS	Clear To Send input from modem, data set, or peripheral device (active low)

3-3-2. UART Interface Functional Description

3-3-2-1. Booting from UART

When booting from the UART, the AW-CM276NF device has the following requirements:

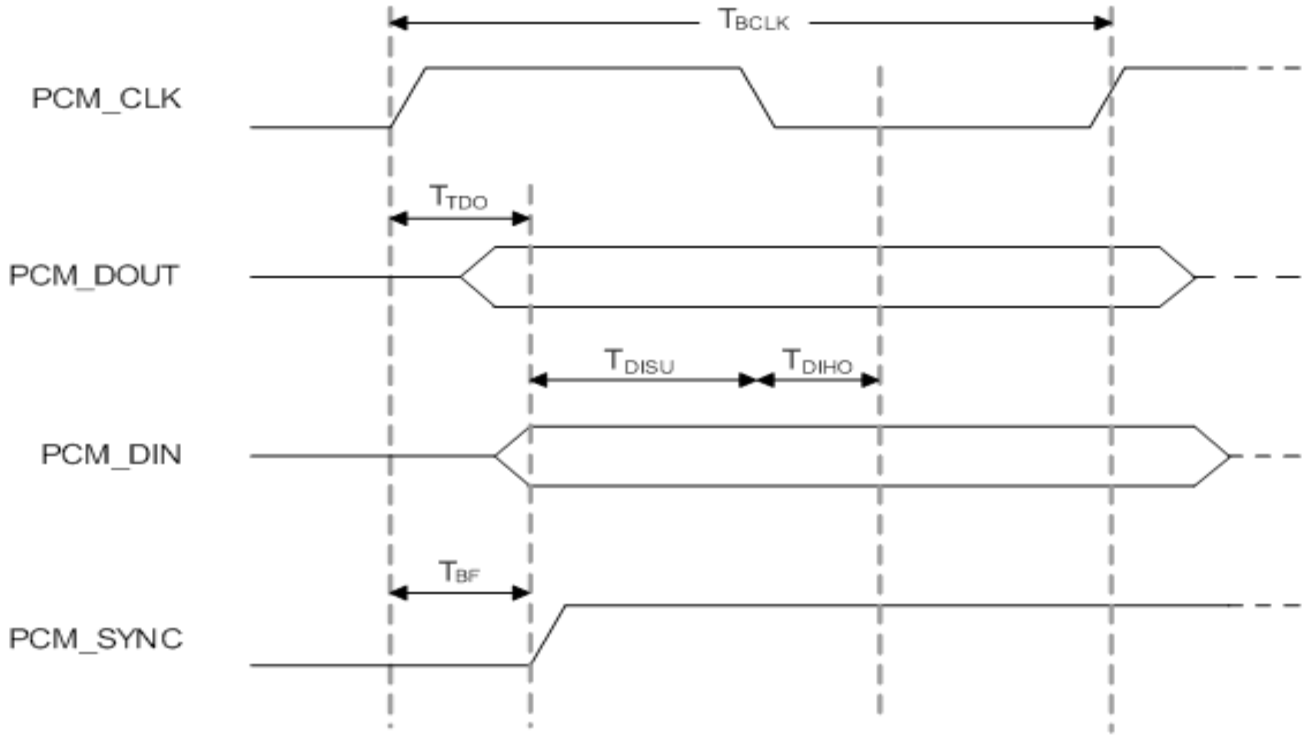
System Requirement	Description
Number of data bits	8 bits
Stop bits	1 bit
Parity	No parity
Baud Rate	115200

3-3-2-2. UART as Test Port

Test diagnostic programs may be uploaded to the CPU through the UART interface. During execution, the diagnostic program transmits performance and status information through the UART by performing a write to the PBU address space designated to the UART.

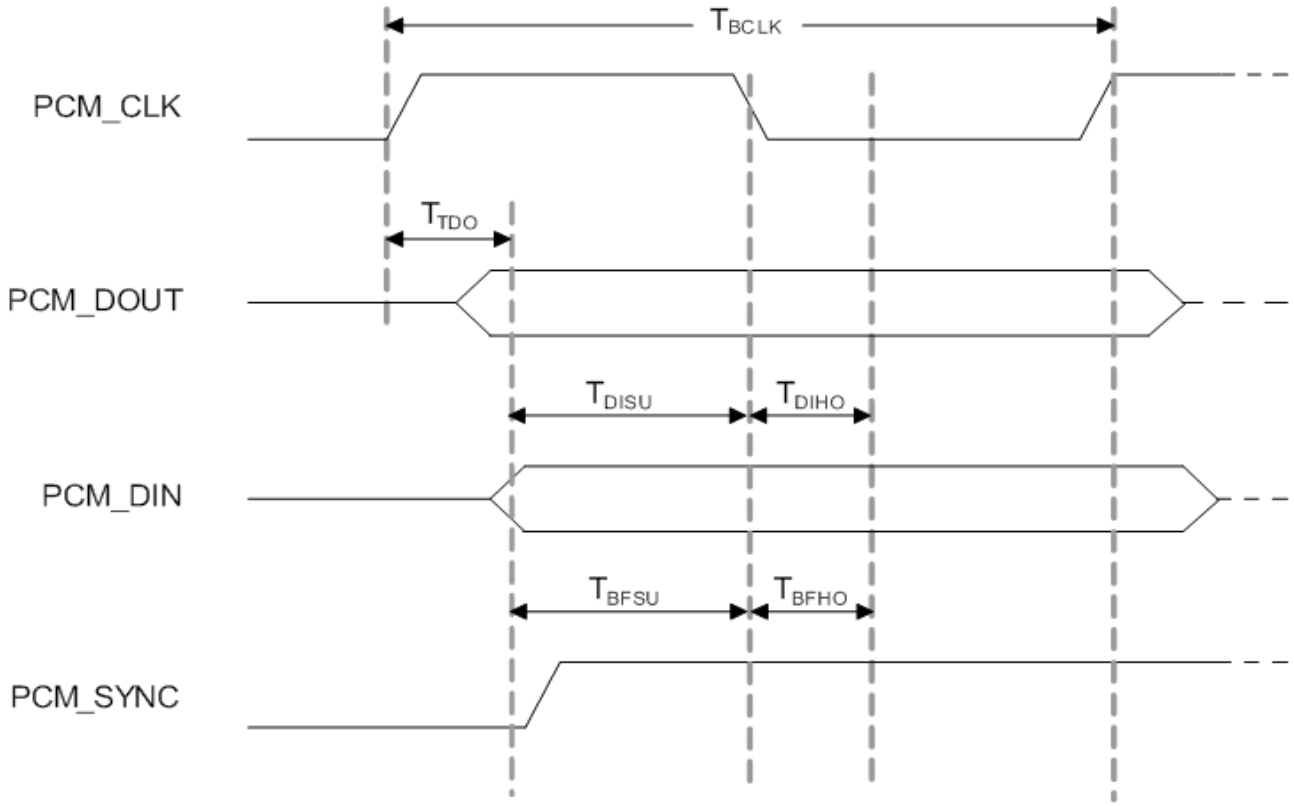
3-4. PCM Interface

3-4-1. PCM Timing Specification – Master Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

3-4-2. PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}	--	--	10	--	--	ns

4. Pin Definition

Pin No	Definition	Basic Description	Type	Supply
1	NC	NC		
2	NC	NC		
3	NC	NC		
4	3.3V	3.3V Power Supply	I	3.3V
5	3.3V	3.3V Power Supply	I	3.3V
6	GND	System Ground Pin		
7	NC	NC		
8	CONFIG_HOST[0]	Configuration: CONFIG_HOST[0]		
9	CONFIG_HOST[1]	Configuration: CONFIG_HOST[1]		
10	CONFIG_HOST[2]	Configuration: CONFIG_HOST[2]		
11	GPIO[17] /UART_LTE_SOUT/TDO	GPIO[17] / UART_LTE_SOUT/TDO (output)	O	VIO
12	GPIO[16]/ UART_LTE_SIN/TDI	GPIO[16] / UART_LTE_SIN/TDI (input)	I	VIO
13	CONFIG_HOST[3]	Configuration: CONFIG_HOST[3]		
14	NC	NC		
15	GPIO[1]	GPIO[1] (input/output)	I/O	VIO
16	NC	NC	I/O	
17	GND	System Ground Pin		
18	GPIO[25]	GPIO[25] (input/output)	I/O	VIO
19	NC	NC		
20	GND	System Ground Pin		
21	GPIO[26]	GPIO[26] (input/output)	I/O	VIO
22	GPIO[27]	GPIO[27] (input/output)	I/O	VIO
23	GND	System Ground Pin		
24	ATEST0	NC, reserved for debug	I	
25	NC	NC	I/O	
26	GND	System Ground Pin		
27	SLP_CLK	Sleep Clock Input Used for WLAN and Bluetooth low- power modes. External sleep clock of 32.768 KHz must be used fo r auto reference clock calibration and for WLAN/Bluetooth low power operation.	I	

Pin No	Definition	Basic Description	Type	Supply
28	GPIO[13]/BT IRQ(O)	GPIO[13]/ BT Wake Host(active low) (output)	O	VIO
29	PCIE_WAKEn	PCIe wake signal (input/output) (active low)	I/O	VIO
30	PCIE_CLKREQn	PCIe clock request (input/output) (active low)	I/O	VIO
31	GPIO[21]/PCIE_PERSTn	PCIe host indication to reset the device (input) (active low)	I	VIO
32	GND	System Ground Pin		
33	PCIE_RCLK_N	PCI Express Differential Clock Input—Negative	I	1.8V(internal)
34	PCIE_RCLK_P	PCI Express Differential Clock Input—Positive	I	1.8V(internal)
35	GND	System Ground Pin		
36	PCIE_TX_N/USB3.0_TX_N	PCI Express Transmit Data—Negative / USB 3.0 TX negative	O	1.8V(internal)
37	PCIE_TX_P/USB3.0_TX_P	PCI Express Transmit Data—Positive / USB 3.0 TX positive	O	1.8V(internal)
38	GND	System Ground Pin		
39	PCIE_RX_N/USB3.0_RX_N	PCI Express Receive Data—Negative / USB 3.0 RX negative	I	1.8V(internal)
40	PCIE_RX_P/USB3.0_RX_P	PCI Express Receive Data—Positive / USB 3.0 RX positive	I	1.8V(internal)
41	GND	System Ground Pin		
42	GPIO[0]/CLK_REQ	GPIO[0] (input/output)	O	VIO
43	NC	NC		
44	VIO_SD	1.8V/3.3V Digital I/O SDIO Power Supply	I	VIO_SD
45	PDn	Full Power Down (input) (active low)	I	3.3V
46	GPIO[14] /TCK/WLAN Wake Host	GPIO[14]/TCK/WLAN Wake Host(active low) (output)	O	VIO
47	SD_DAT[3]	SDIO Data line Bit[3]	I/O	VIO_SD
48	SD_DAT[2]	SDIO Data line Bit[2]	I/O	VIO_SD
49	SD_DAT[1]	SDIO Data line Bit[1]	I/O	VIO_SD
50	SD_DAT[0]	SDIO Data line Bit[0]	I/O	VIO_SD
51	SD_CMD	SDIO Command/response (input/output)	I/O	VIO_SD
52	SD_CLK	SDIO Clock input	I	VIO_SD
53	GPIO[12] / UART Host Wake BT	GPIO[12]/ UART Host Wake BT(active low) (input)	I	VIO
54	GPIO[10] / UART_CTSn	GPIO[10 / UART_CTSn] (input)	I	VIO
55	GPIO[8] / UART_SOUT	GPIO[8] / UART_SOUT (output)	O	VIO
56	GPIO[9] / UART_SIN	GPIO[9] / UART_SIN (input)	I	VIO
57	GPIO[11] / UART_RTSn	GPIO[11] / UART_RTSn (output)	O	VIO
58	GPIO[7] / PCM_SYNC	GPIO[7] / PCM_SYNC (input/output)	I/O	VIO

Pin No	Definition	Basic Description	Type	Supply
59	GPIO[4] / PCM_IN	GPIO[4] / PCM_IN (input)	I	VIO
60	GPIO[5] / PCM_OUT	GPIO[5] / PCM_OUT (output)	O	VIO
61	GPIO[6] / PCM_CLK	GPIO[6] / PCM_CLK (input)	I	VIO
62	GND	System Ground Pin		
63	GPIO[22] / PCIE_W_DISABLEn	GPIO[22] / PCIE_W_DISABLEn (input)	I	VIO
64	GPIO[2] / WLAN_LED	LED_OUT_WLAN (output)	O	VIO
65	GPIO[3] / BT_LED	LED_OUT_BT (output)	O	VIO
66	GPIO[15] / TMS/ Host Wake WLAN	GPIO[15] / JTAG TMS/ Host Wake WLAN (input)	I	VIO
67	NC	NC		
68	GND	System Ground Pin		
69	USB_DM	USB Serial Differential Data Minus	I/O	3.3V
70	USB_DP	USB Serial Differential Data Plus	I/O	3.3V
71	GND	System Ground Pin		
72	3.3V	3.3V Power Supply	I	3.3V
73	VIO	Digital I/O Power Supply	I	VIO
74	GND	System Ground Pin		
75	GND	System Ground Pin		
76	GND	System Ground Pin		
77	GND	System Ground Pin		
78	GND	System Ground Pin		
79	GND	System Ground Pin		
80	GND	System Ground Pin		
81	GND	System Ground Pin		
82	GND	System Ground Pin		
83	GND	System Ground Pin		
84	GND	System Ground Pin		
85	GND	System Ground Pin		
86	GND	System Ground Pin		
87	GND	System Ground Pin		
88	GND	System Ground Pin		
89	GND	System Ground Pin		

Pin No	Definition	Basic Description	Type	Supply
90	GND	System Ground Pin		
91	GND	System Ground Pin		
92	GND	System Ground Pin		
93	GND	System Ground Pin		
94	GND	System Ground Pin		
95	GND	System Ground Pin		
96	GND	System Ground Pin		
G1	GND	System Ground Pin		
G2	GND	System Ground Pin		
G3	GND	System Ground Pin		
G4	GND	System Ground Pin		
G5	GND	System Ground Pin		
G6	GND	System Ground Pin		
G7	GND	System Ground Pin		
G8	GND	System Ground Pin		
G9	GND	System Ground Pin		
G10	GND	System Ground Pin		
G11	GND	System Ground Pin		
G12	GND	System Ground Pin		
G13	GND	System Ground Pin		
G14	GND	System Ground Pin		
G15	GND	System Ground Pin		
G16	GND	System Ground Pin		
G19	GND	System Ground Pin		
G20	GND	System Ground Pin		
G21	GND	System Ground Pin		
G22	GND	System Ground Pin		
G23	GND	System Ground Pin		
G24	GND	System Ground Pin		
G25	GND	System Ground Pin		

Pin No	Definition	Basic Description	Type	
G26	GND	System Ground Pin		
G27	GND	System Ground Pin		
G28	GND	System Ground Pin		
G29	GND	System Ground Pin		
G30	GND	System Ground Pin		
G31	GND	System Ground Pin		
G32	GND	System Ground Pin		
G33	GND	System Ground Pin		
G34	GND	System Ground Pin		
G35	GND	System Ground Pin		
G36	GND	System Ground Pin		

Notes:

1. PCIE Impedance targets: Single-ended Z of 60 ohms +- 15% . Differential Impedance of ~100 ohm +- 20%.
2. USB Impedance targets: D+/D- are differential and should have 90ohms impedance.
3. * Implement by different hardware version.

Note: Interface supports and combinations as shown below:

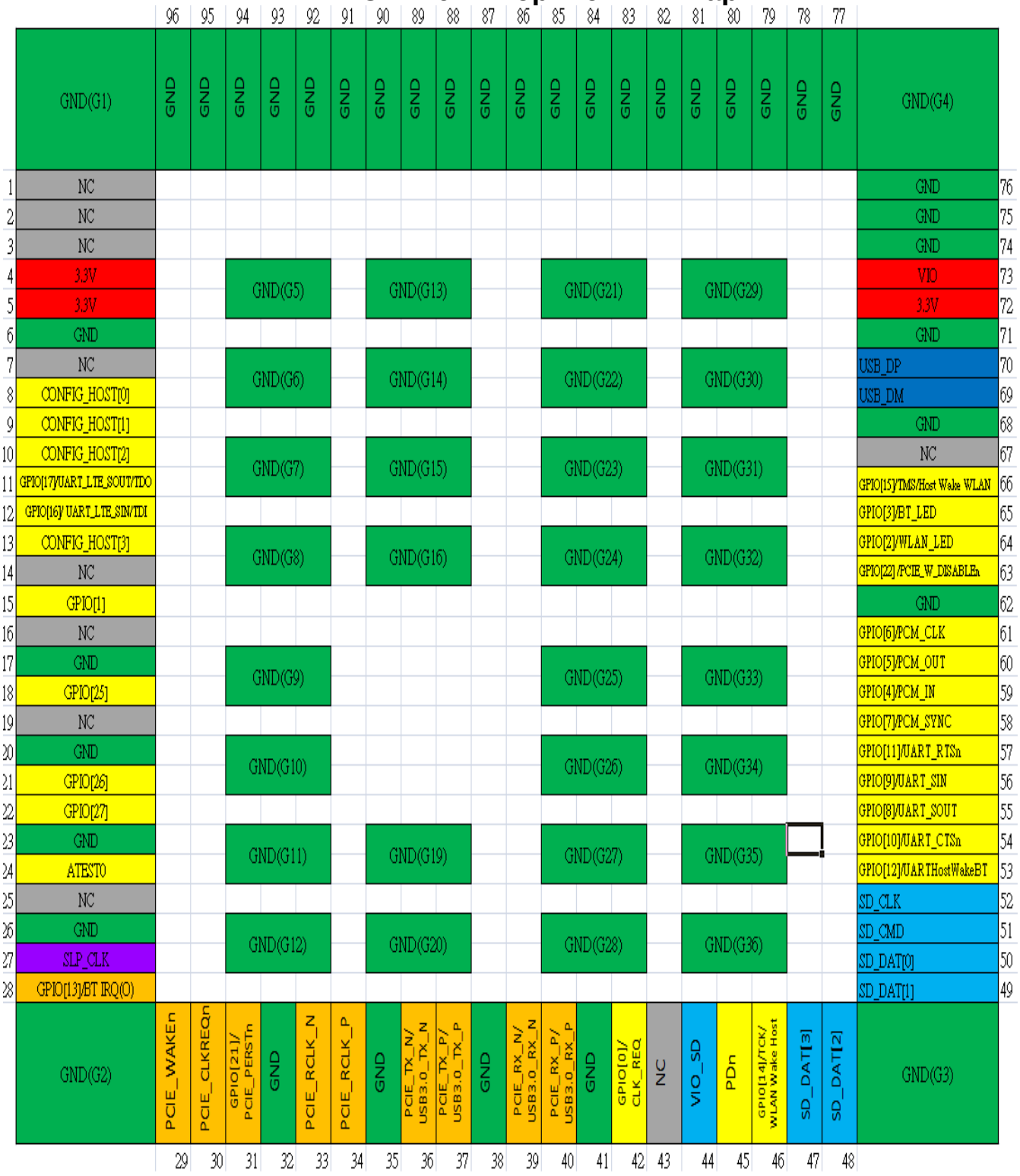
Scenario	WLAN	BT	Strap value CON[2:0]
1	SDIO	UART	000
2	SDIO	SDIO	001
3	PCIe	USB	010(default)
4	PCIe	UART	011
5	USB3.0	UART	100
6	USB2.0	USB2.0	101
7	USB3/2.0	USB3/2.0	110
8	USB3.0	USB3.0	111

*Configuration pins:

Pin No.	Configuration
10	CON[2]
9	CON[1]
8	CON[0]

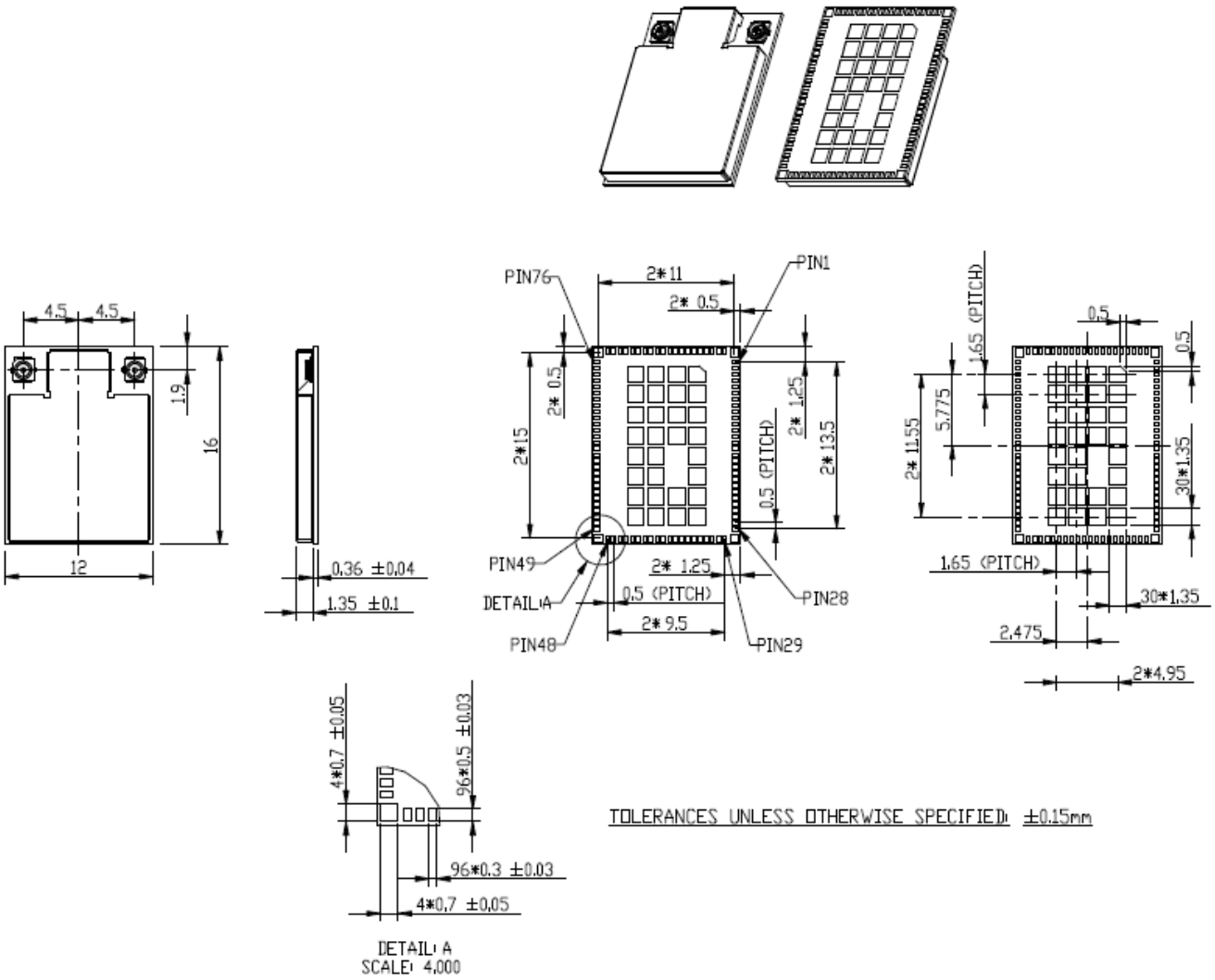
5. Pin map

AW-CM276NF Top View Pin Map

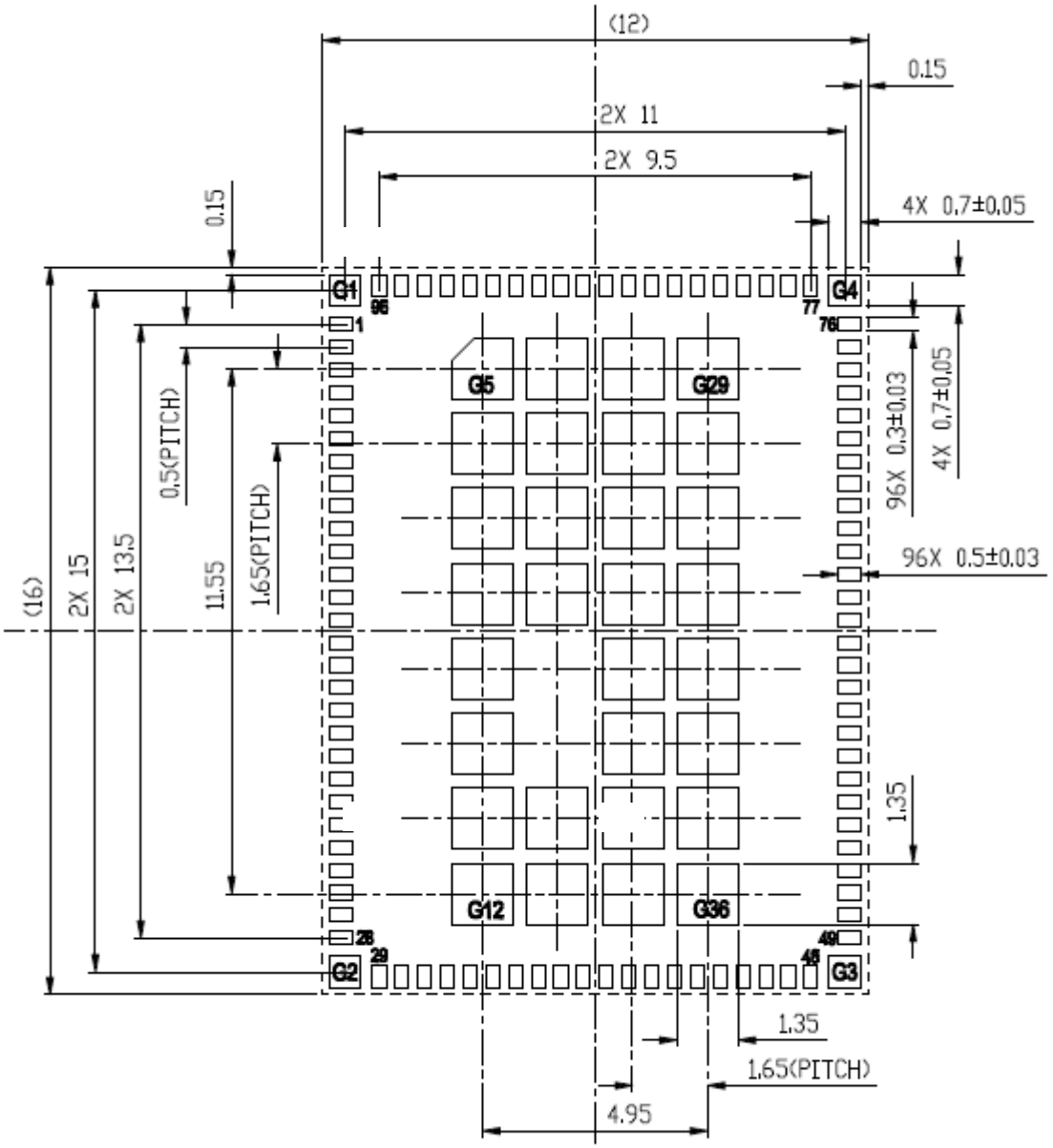


6. Mechanical Information

6-1. Package Outline Drawing

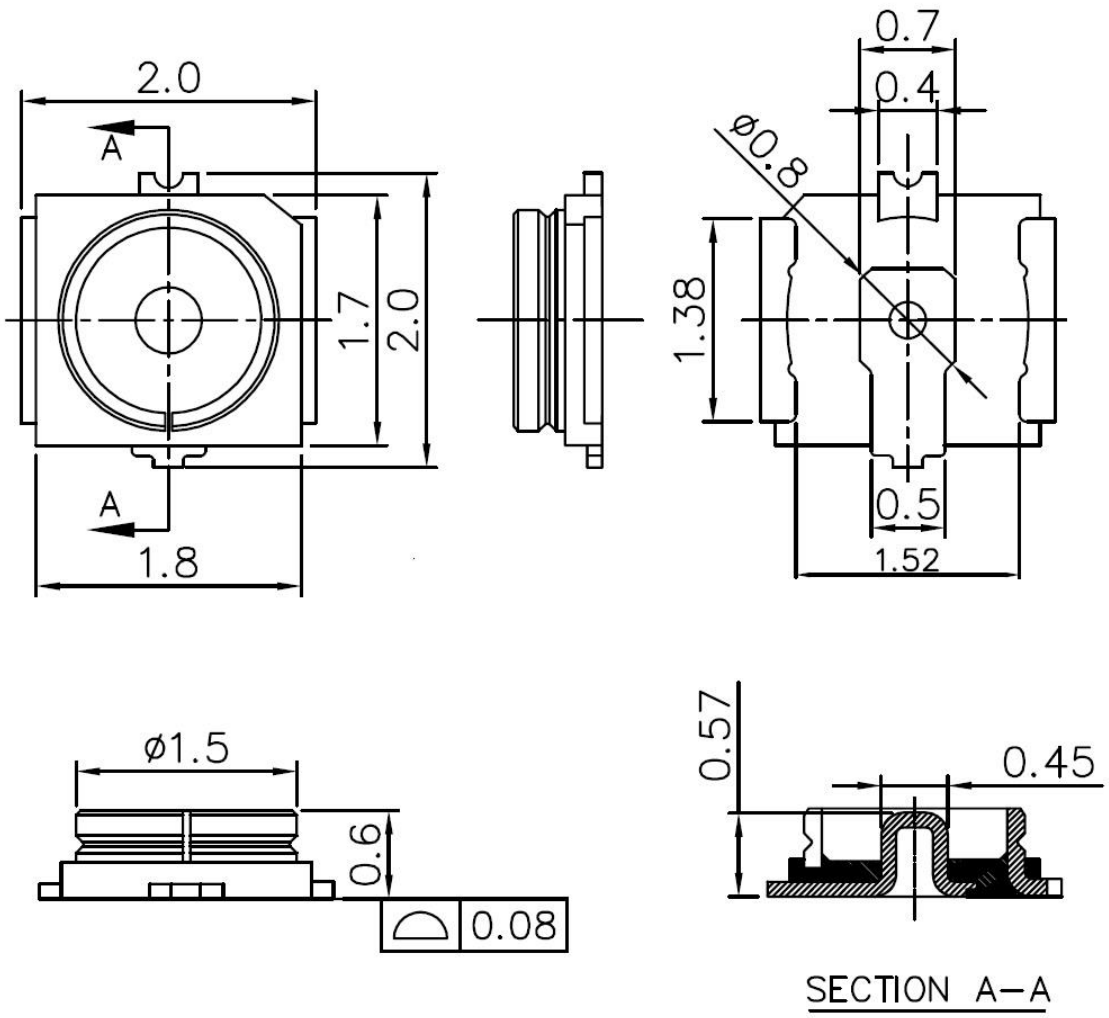


6-2. Pin out drawing



RECOMMENDED SOLDER PAD LAYOUT

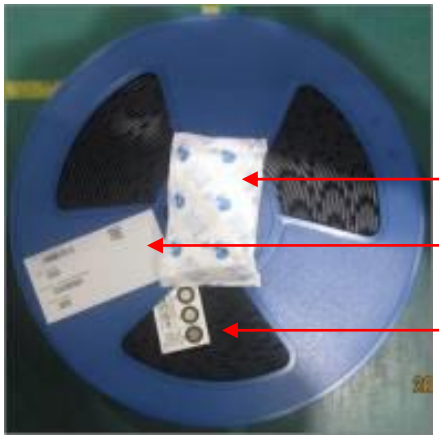
6-3. Antenna Connector Drawing



UNITS: mm

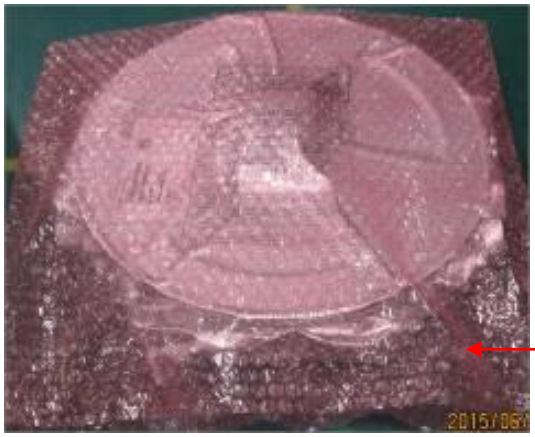
7. Shipping Information

7-1



7-2

7-3



7-4

7-5

1 Carton= 5 Boxes

7-6

Note: 1 tape reel = 1 box = 1,500pcs

1 carton = 5 boxes = 5 * 1,500pcs=7,500pcs