

# **AW-XM369**

## **IEEE 802.11 2X2 WiFi 6 SU and MU-MIMO DBC Wireless LAN + Bluetooth 5 Combo LGA Module**

### **Datasheet**

**Rev. A**

**DF**

**For Standard**

## Features

### WLAN

- ◆ Support 2x2 802.11 a/b/g/n/ac/ax
- ◆ Dual bands: 2.4 GHz and 5 GHz
  - ◆ Support 20/40/80/(80+80) MHz channel Bandwidths.
- ◆ 5GHz PHY data rates up to 1.2 Gbps
- ◆ 2.4 GHz PHY data rates up to 458 Mbps
- ◆ Uplink and downlink OFDMA and MU-MIMO
- ◆ Instantaneous 0-DFS

### WLAN Dual-Radios

- ◆ Dual, independent direct-conversion WLAN radios (with dual-MACs and dual-Basebands) supports true, simultaneous WLAN network operation at 2 different frequency bands,

### Bluetooth

- ◆ Bluetooth 5
- ◆ Bluetooth class 2
- ◆ Bluetooth class 1
- ◆ PCM interface for voice applications
- ◆ 2Mbit/s LE
- ◆ Long range
- ◆ LTE/MWS coexistence
- ◆ 2 x wide band speech (WBS) calls
- ◆ Security: AES

## Revision History

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Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/01/21		<ul style="list-style-type: none"> <li>Draft version</li> </ul>	Renton Tao	N.C Chen

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# 1. Introduction

## 1.1 Product Overview

**AzureWave Technologies, Inc.** introduces the IEEE 802.11a/b/g/n/ac/ax Concurrent Dual WiFi(CDW) and BT, combo module – **AW-XM369**. With High Efficiency Wireless(HEW) and backward compatible with 802.11ac technologies integrated into a module, AW-XM369 provides the best and most convenient SMT process. The module is targeted to mobile devices including, Tablet PC, Portable Media Players (PMPs), Portable Navigation Devices (PNDs), Personal Digital Assistants (PDAs), Tracking Devices, Gaming Devices which need convenient SMT process, low power consumption.

By using AW-XM369, the customers can easily integrate the Wi-Fi, BT, by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11a/b/g/n/ac/ax standard, the AW-XM369 uses **DSSS, OFDM, DBPSK, DQPSK, CCK and QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-XM369.

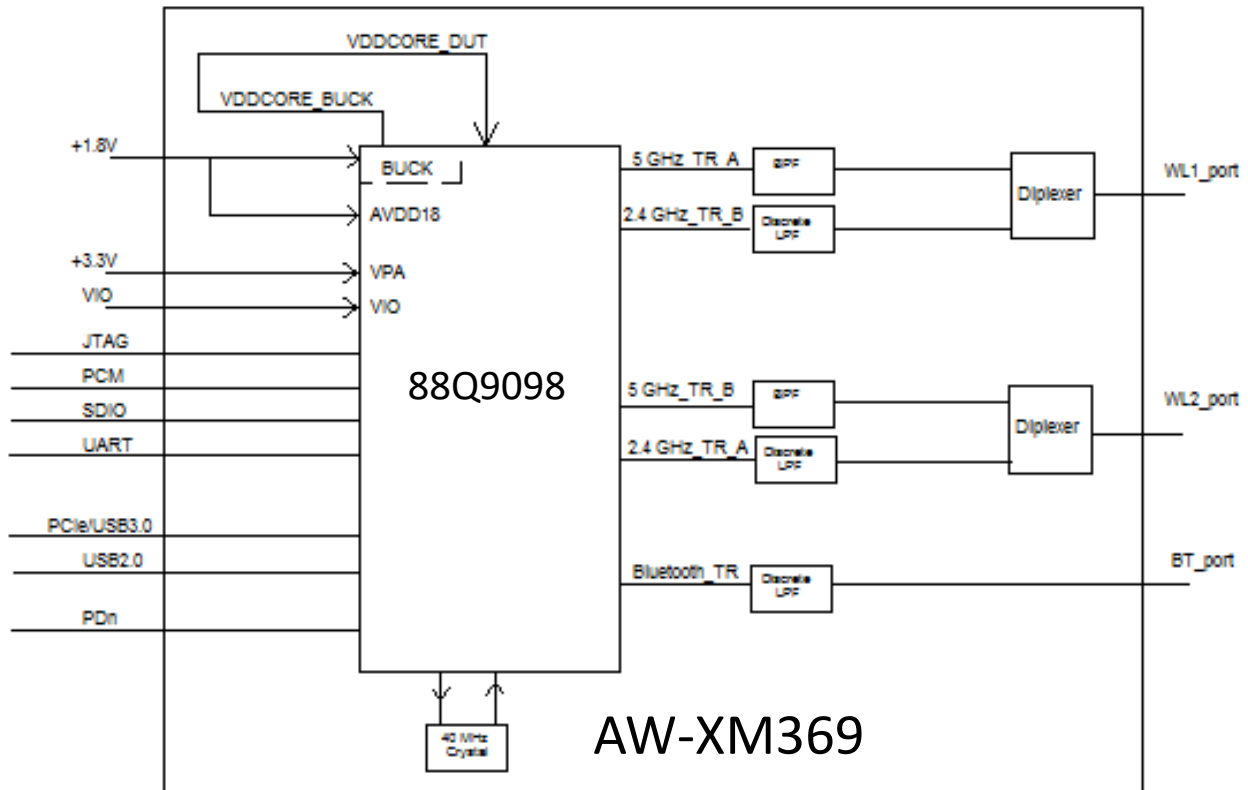
The AW-XM369 supports standard interface **PCIe, SDIO, and USB2.0/3.0 for WLAN** interface connection. High-Speed **UART, SDIO, and USB2.0/3.0for BT** interface connection. AW-XM369 is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the AW-XM369 is the best solution for the consumer electronics and the tablet PC.

Scenario	2.4GHz Band			5GHz Band		
	Mode	Technology	BW	Mode	Technology	BW
1	2x2	802.11n	40MHz	2x2	802.11ax	80MHz
2	2x2	802.11n	40MHz	1x1	802.11ax	80+80MHz
3	2x2	802.11ax	40MHz	2x2	802.11ac	40MHz
4	2x2	802.11n	40MHz	1x1	802.11ax	80MHz

Concurrent 2.4GHz and 5GHz modes supported table

## 1.2 Block Diagram

A simplified block diagram of the AW-XM369 module is depicted in the figure below.



v

## 1.3 Specifications Table

### 1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi with Bluetooth 5 Combo Module
Major Chipset	NXP 88Q9098
Host Interface	Wi-Fi: PCIe3.0, SDIO3.0, USB2.0/3.0, BT: SDIO3.0, UART, USB2.0/3.0
Dimension	20 mm X 18 mm x 2.85 mm(Max)
Package	LGA
Weight	TBD

### 1.3.2 WLAN

Features	Description
WLAN Standard	IEEE802.11 a/b/g/n/ac/ax
Frequency Range	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM
Number of Channels	2.4GHz: <ul style="list-style-type: none"> <li>■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11</li> <li>■ China, Australia, Most European Countries - 1 ~ 13</li> <li>■ Japan, 1 ~ 13</li> </ul> 5GHz: <ul style="list-style-type: none"> <li>■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165</li> <li>■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140</li> <li>■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</li> </ul>

Output Power  
(Board Level Limit)\*

### 2.4G

	Min	Typ	Max	Unit
11b (11Mbps) @EVM<35%		18		dBm
11g (54Mbps) @EVM $\leq$ -27 dB		17		dBm
11n (HT20 MCS7) @EVM $\leq$ -28 dB		16		dBm
11n (HT40 MCS7) @EVM $\leq$ -28 dB		16		dBm
11n (HE20 MCS11) @EVM $\leq$ -35 dB		TBD		dBm
11n (HE40 MCS11) @EVM $\leq$ -35 dB		TBD		dBm

### 5G

	Min	Typ	Max	Unit
11a (54Mbps) @EVM $\leq$ -27 dB		16		dBm
11n (HT20 MCS7) @EVM $\leq$ -28 dB		16		dBm
11n (HT40 MCS7) @EVM $\leq$ -28 dB		15		dBm
11ac(VHT20 MCS8) @EVM $\leq$ -31 dB		15		dBm
11ac(VHT40 MCS9) @EVM $\leq$ -32 dB		15		dBm
11ac(VHT80 MCS9) @EVM $\leq$ -32 dB		15		dBm
11ax(HE20 MCS11) @EVM $\leq$ -35 dB		TBD		dBm
11ax(HE40 MCS11) @EVM $\leq$ -35 dB		TBD		dBm
11ax(HE80 MCS11) @EVM $\leq$ -35 dB		TBD		dBm

Receiver Sensitivity	<b>2.4G</b>				
		Min	Typ	Max	Unit
	11b (11Mbps)	-	-88		dBm
	11g (54Mbps)	-	-75		dBm
	11n (HT20 MCS7)	-	-72		dBm
	11n (HT40 MCS7)	-	-69		dBm
	11ax(HE20 MCS11)		TBD		dBm
	11ax(HE40 MCS11)		TBD		dBm
	<b>5G</b>				
		Min	Typ	Max	Unit
	11a (54Mbps)	-	-72		dBm
	11n (HT20 MCS7)	-	-70		dBm
	11n (HT40 MCS7)	-	-68		dBm
	11ac(VHT20 MCS8)	-	-65		dBm
	11ac(VHT40 MCS9)		-63		dBm
11ac(VHT80 MCS9)		-60		dBm	
11ax(HE20 MCS11)		TBD		dBm	
11ax(HE40 MCS11)		TBD		dBm	
11ax(HE80 MCS11)		TBD		dBm	
Data Rate	<ul style="list-style-type: none"> <li>■ 802.11b: 1, 2, 5.5, 11Mbps</li> <li>■ 802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps</li> <li>■ 802.11n: up to 150Mbps-single</li> <li>■ 802.11n: up to 300Mbps-2x2 MIMO</li> <li>■ 802.11ac: up to 192.6Mbps (20MHz channel)</li> <li>■ 802.11ac: up to 400Mbps (40MHz channel)</li> <li>■ 802.11ac: up to 866.7Mbps (80MHz channel)</li> <li>■ 802.11ax: 2.4GHz up to 458Mbps, 5GHz up to 1.2Gbps</li> </ul>				
Security	<ul style="list-style-type: none"> <li>■ WiFi: WPA/WPA3</li> </ul>				

\* If you have any certification questions about output power please contact FAE directly.

### 1.3.3 Bluetooth

Features	Description
Bluetooth Standard	Full Bluetooth 5 features
Frequency Range	2402MHz~2483MHz

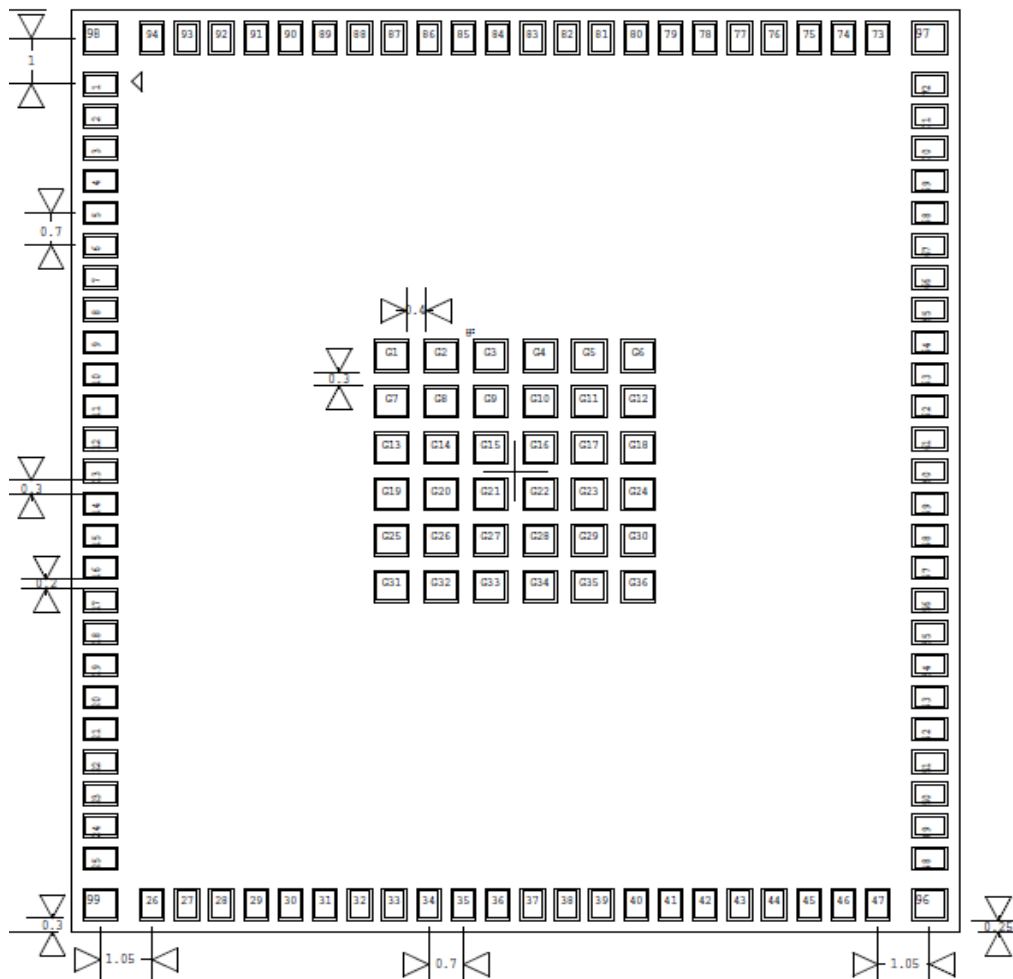
Modulation	Header GFSK Payload 2M: $\pi/4$ -DQPSK Payload 3M: 8DPSK				
Output Power		Min	Typ	Max	Unit
	BDR		TBD		dBm
	EDR		TBD		dBm
	Low Energy		TBD		dBm
Receiver Sensitivity	BT Sensitivity (BER<0.1%)				
		Min	Typ	Max	Unit
	BDR(DH1)	-	TBD		dBm
	EDR(2DH5)	-	TBD		dBm
	EDR(3DH5)	-	TBD		dBm
Low Energy	-	TBD		dBm	

### 1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V +-5%
Operating Temperature	-40 ~ +85 °C
Operating Humidity	<85% (non condensing)
Storage Temperature	-55 ~ +125 °C
Storage Humidity	<60% (non condensing)
ESD Protection	
Human Body Model	TBD
Changed Device Model	TBD

## 2.1 Pin Map

AW-XM369 pin out drawing (top view).



## 2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GPIO[5]	GPIO Mode : GPIO[5].	VDDIO	I/O
2	GPIO[4]	GPIO Mode : GPIO[4].	VDDIO	I/O
3	GPIO[1]	GPIO Mode : GPIO[1].	VDDIO	I/O
4	GND	Ground	---	---
5	PCIE_RCLK_P	PCI Express Differential Clock Input—Positive	1V8	I
6	PCIE_RCLK_N	PCI Express Differential Clock Input—Negative	1V8	I
7	GND	Ground	---	---
8	PCIE_TX_P/USB3.0_TX_P	PCI Express Transmit Data—Positive / USB 3.0 TX positive	1V8	O
9	PCIE_TX_N/USB3.0_TX_N	PCI Express Transmit Data—Negative / USB 3.0 TX negative	1V8	O
10	GND	Ground	---	---
11	PCIE_RX_N/USB3.0_RX_N	PCI Express Receive Data—Negative / USB 3.0 RX negative	1V8	I
12	PCIE_RX_P/USB3.0_RX_P	PCI Express Receive Data—Positive / USB 3.0 RX positive	1V8	I
13	GND	Ground	---	---
14	USB_DM	USB Serial Differential Data Minus	3V3	I/O
15	USB_DP	USB Serial Differential Data Plus	3V3	I/O
16	GND	Ground	---	---
17	SD_DAT[3]	SDIO Data line Bit[3]	VIO_SD	I/O
18	SD_DAT[2]	SDIO Data line Bit[2]	VIO_SD	I/O
19	SD_DAT[1]	SDIO Data line Bit[1]	VIO_SD	I/O
20	SD_DAT[0]	SDIO Data line Bit[0]	VIO_SD	I/O
21	SD_CMD	SDIO Command/response (input/output)	VIO_SD	I/O
22	SD_CLK	SDIO Clock input	VIO_SD	I
23	VIO_SD	1.8V/3.3V Digital I/O SDIO Power Supply	1.8 or 3.3V	I
24	GND	Ground	---	---
25	PCIE_PERSTn	PCIe host indication to reset the device (active low)	VIO	I
26	PCIE_CLKREQn	PCIe clock request (active low)	VIO	I/O
27	PCIE_WAKEn	PCIe wake signal (active low)	VIO	I/O
28	PCIE_DISABLEn	PCIe DISABLEn(active low)	VIO	I
29	GND	Ground	---	---
30	UART_RTSn	UART Mode: UART_RTSn (active low)	VDDIO	O
31	UART_CTSn	UART Mode: UART_CTSn (active low)	VDDIO	I
32	UART_RX	UART SIN pin	VDDIO	I
33	UART_TX	UART SOUT.pin	VDDIO	O
34	GPIO[12]	GPIO Mode : GPIO[12].	VDDIO	I/O
35	GPIO[13]	GPIO Mode : GPIO[13].	VDDIO	I/O
36	NC	NC	---	floating
37	NC	NC	---	floating

38	NC	NC	---	floating
39	NC	NC	---	floating
40	NC	NC	---	floating
41	NC	NC	---	floating
42	NC	NC	---	floating
43	NC	NC	---	floating
44	NC	NC	---	floating
45	NC	NC	---	floating
46	NC	NC	---	floating
47	NC	NC	---	floating
48	BT_ANT	RF I/O pad for BT	---	I/O
49	GND	Ground	---	---
50	GND	Ground	---	---
51	GND	Ground	---	---
52	WLAN_ANT_2	RF I/O pad for WLAN ANT 2	---	I/O
53	GND	Ground	---	---
54	GND	Ground	---	---
55	GND	Ground	---	---
56	GND	Ground	---	---
57	GND	Ground	---	---
58	GND	Ground	---	---
59	GND	Ground	---	---
60	GND	Ground	---	---
61	GND	Ground	---	---
62	GND	Ground	---	---
63	GND	Ground	---	---
64	GND	Ground	---	---
65	GND	Ground	---	---
66	GND	Ground	---	---
67	GND	Ground	---	---
68	GND	Ground	---	---
69	WLAN_ANT_2	RF I/O pad for WLAN ANT 2	---	I/O
70	3V3	3.3V DC power supply	3.3V	I
71	3V3	3.3V DC power supply	3.3V	I
72	GND	Ground	---	---
73	CON[0]	Firmware Boot Options. See below table*	VIO	I
74	CON[1]	Firmware Boot Options. See below table*	VIO	I
75	CON[2]	Firmware Boot Options. See below table*	VIO	I
76	NC	NC	---	floating
77	NC	NC	---	floating
78	NC	NC	---	floating
79	NC	NC	---	floating
80	NC	NC	---	floating
81	NC	NC	---	floating

82	NC	NC	---	floating
83	GND	Ground	---	---
84	PDn	Full Power-down input pin (active low) 0 = full power-down mode 1 = normal mode	3V3	I
85	GPIO[0]	GPIO Mode : GPIO[0].	VDDIO	I/O
86	GPIO[14]	GPIO Mode : GPIO[14].	VDDIO	I/O
87	GPIO[15]	GPIO Mode : GPIO[15].	VDDIO	I/O
88	GPIO[16]	GPIO Mode : GPIO[16].	VDDIO	I/O
89	GPIO[17]	GPIO Mode : GPIO[17].	VDDIO	I/O
90	VIO	Digital I/O power supply	1.8 or 3.3V	I
91	GND	Ground	---	---
92	1V8	1.8V DC power supply	1.8V	I
93	1V8	1.8V DC power supply	1.8V	I
94	GPIO[6]	GPIO Mode : GPIO[6].	VDDIO	I/O
95	GND	Ground	---	---
96	GND	Ground	---	---
97	GND	Ground	---	---
98	GND	Ground	---	---
G1~36	GND	Ground	---	---

\*Firmware Boot options

Strap Value	WLAN	Bluetooth/LE
000	SDIO	UART
001	SDIO	SDIO
010	PCIe	PCIe
011	PCIe	UART
100	USB3/2	UART
101	reserved	reserved
110	USB3/2	USB3/2
111	PCIe	USB2

### 3. Electrical Characteristics

#### 3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3V3	DC supply for the 3.3V input	-	3.3	3.63	V
1V8	DC supply for the 1.8V input		1.8	2.16	
VIO	I/O power supply	-	3.3	3.63	V
		-	1.8	1.98	
VIO_SD	SDIO power supply	-	3.3	3.63	V
		-	1.8	1.98	

#### 3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3.3V	DC supply for the 3.3V input	3.14	3.3	3.46	V
1V8	DC supply for the 1.8V input	1.71	1.8	1.89	V
VIO	1.8V/3.3V digital I/O power supply	3.14	3.3	3.46	V
		1.71	1.8	1.89	
VIO_SD	1.8V/3.3V SDIO power supply	3.14	3.3	3.46	V
		1.71	1.8	1.89	

#### 3.3 Digital IO Pin DC Characteristics

##### 3.3.1 1.8V Operation (VIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V <sub>IH</sub>	Input high voltage	0.7*VIO	-	VIO+0.4	V
V <sub>IL</sub>	Input low voltage	-0.4	-	0.3*VIO	
V <sub>OH</sub>	Output high voltage	VIO-0.4	-	-	
V <sub>OL</sub>	Output low voltage	-	-	0.4	
V <sub>HYS</sub>	Input Hysteresis	100			mV

### 3.3.2 3.3V Operation (VIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V <sub>IH</sub>	Input high voltage	0.7*VIO	-	VIO+0.4	V
V <sub>IL</sub>	Input low voltage	-0.4	-	0.3*VIO	
V <sub>OH</sub>	Output High Voltage	VIO-0.4	-	-	
V <sub>OL</sub>	Output Low Voltage	-	-	0.4	
V <sub>HYS</sub>	Input Hysteresis	100			mV

### 3.3.3 1.8V Operation (VIO\_SD)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V <sub>IH</sub>	Input high voltage	0.7*VIO_SD	-	VIO_SD+0.4	V
V <sub>IL</sub>	Input low voltage	-0.4	-	0.3*VIO_SD	
V <sub>OH</sub>	Output High Voltage	VIO_SD-0.4	-	-	
V <sub>OL</sub>	Output Low Voltage	-	-	0.4	
V <sub>HYS</sub>	Input Hysteresis	100			mV

### 3.3.4 3.3V Operation (VIO\_SD)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V <sub>IH</sub>	Input high voltage	0.7*VIO_SD	-	VIO_SD+0.4	V
V <sub>IL</sub>	Input low voltage	-0.4	-	0.3* VIO_SD	
V <sub>OH</sub>	Output High Voltage	VIO_SD-0.4	-	-	
V <sub>OL</sub>	Output Low Voltage	-	-	0.4	
V <sub>HYS</sub>	Input Hysteresis	100			mV

### 3.4 Host Interface

#### 3.4.1 SDIO Interface

The AW-XM369 supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-XM369 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

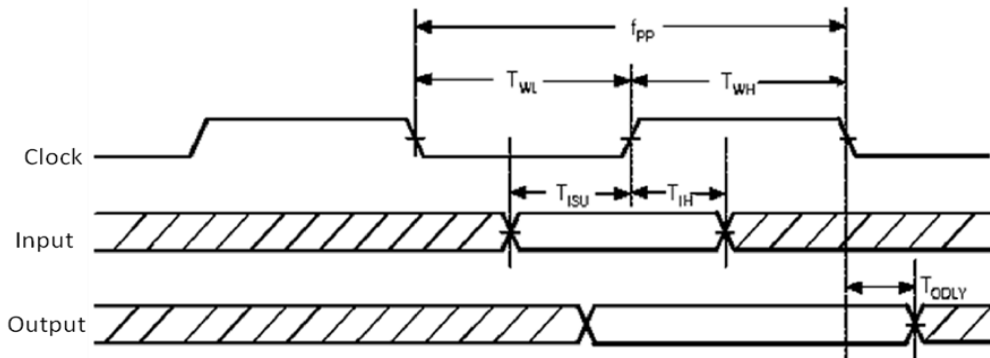
- ◆ Support SDIO 3.0 Standard.
- ◆ On-chip memory used for CIS.
- ◆ Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- ◆ Special interrupt register for information exchange.
- ◆ Allows card to interrupt host.

#### SDIO Interface Signals

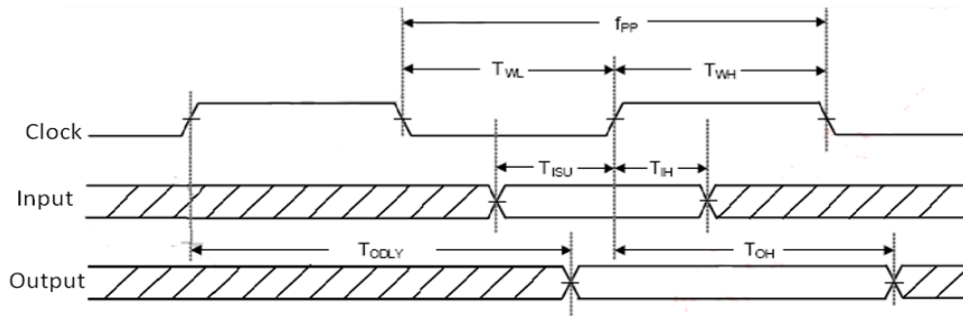
AW-XM369 SDIO Pin Name	Type	Description
SDIO_DATA_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_DATA_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA_3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA_2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA_1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA_0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

### 3.4.2 SDIO Protocol Timing

#### 3.4.2.1 Default Speed, High-Speed Modes (3.3V)



SDIO protocol timing Diagram - Default mode. (3.3V)

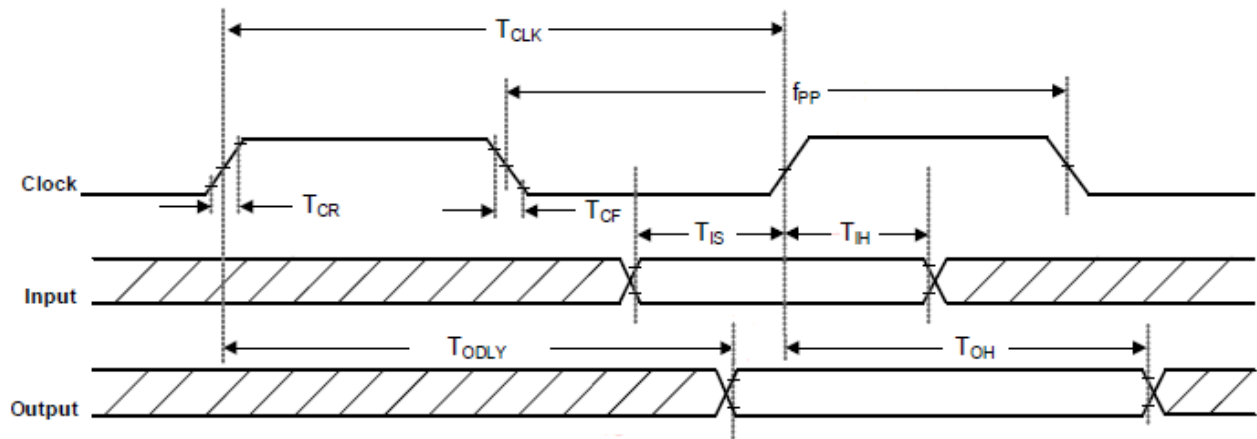


SDIO protocol timing Diagram - High Speed mode. (3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f <sub>pp</sub>	CLK Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T <sub>WH</sub>	CLK High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T <sub>WL</sub>	CLK Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T <sub>ISU</sub>	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
T <sub>IH</sub>	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
T <sub>ODLY</sub>	Output Delay Time	Normal	--	--	14	ns
	CL ≤ 40pF (1 card)	High Speed	--	--	14	ns
T <sub>OH</sub>	Output Hold Time	High Speed	2.5	--	--	ns

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)

### 3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)



SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$F_{pp}$	CLK Frequency	SDR12/25/50	25	-	100	MHz
$T_{CLK}$	Clock Time	SDR12/25/50	10	-	40	ns
$T_{IS}$	Input Setup Time	SDR12/25/50	3	-	-	ns
$T_{IH}$	Input Hold Time	SDR12/25/50	0.8	-	-	ns
$T_{CR}, T_{CF}$	Rise time, fall time TCR, TCF < 2ns(max) at 100MHz CCARD = 10pF	SDR12/25/50	-	-	$0.2 \cdot T_{CLK}$	ns
$T_{ODLY}$	Output Delay Time CL ≤ 30pF	SDR12/25/50	-	-	7.5	ns
$T_{OH}$	Output Hold Time CL = 15pF	SDR12/25/50	1.5	-	-	ns

SDIO Timing Data - SDR12/25/50 modes. (1.8V)

### 3.4.2.3 SDR104 Mode (208MHz) (1.8V)

SDIO Protocol Timing Diagram –SDR104 Mode (208MHz)

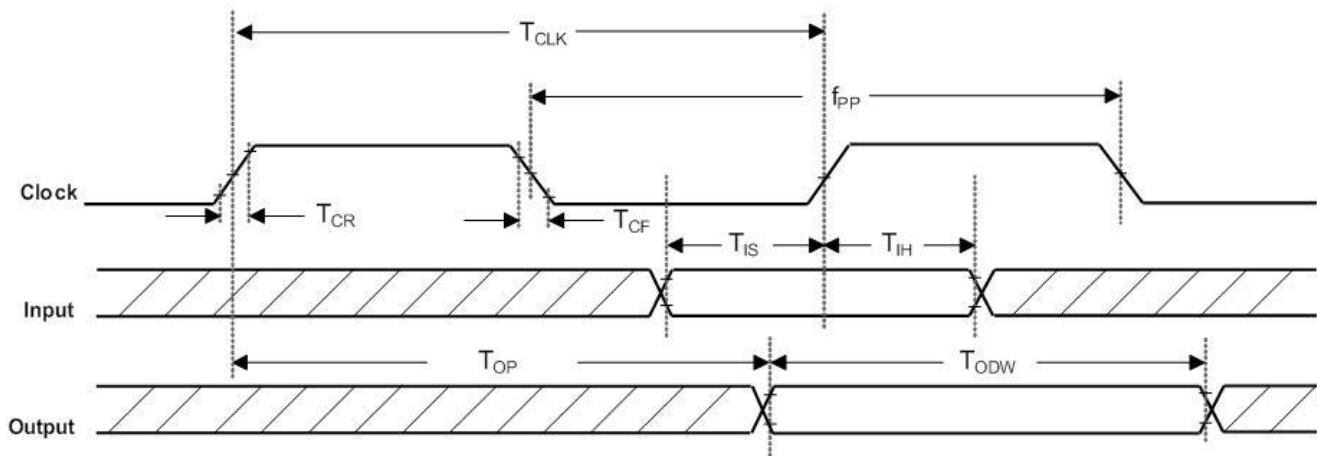
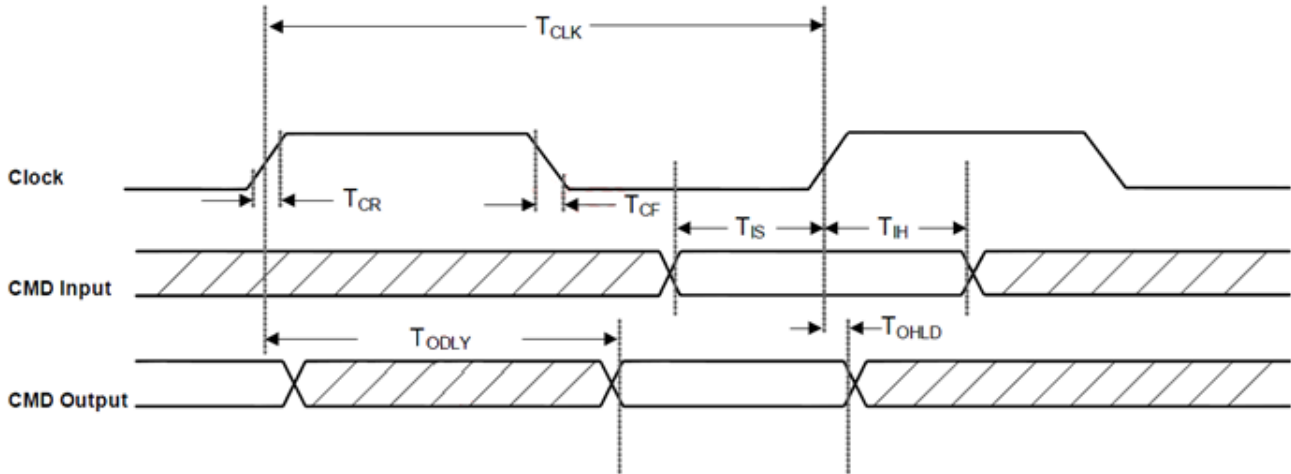


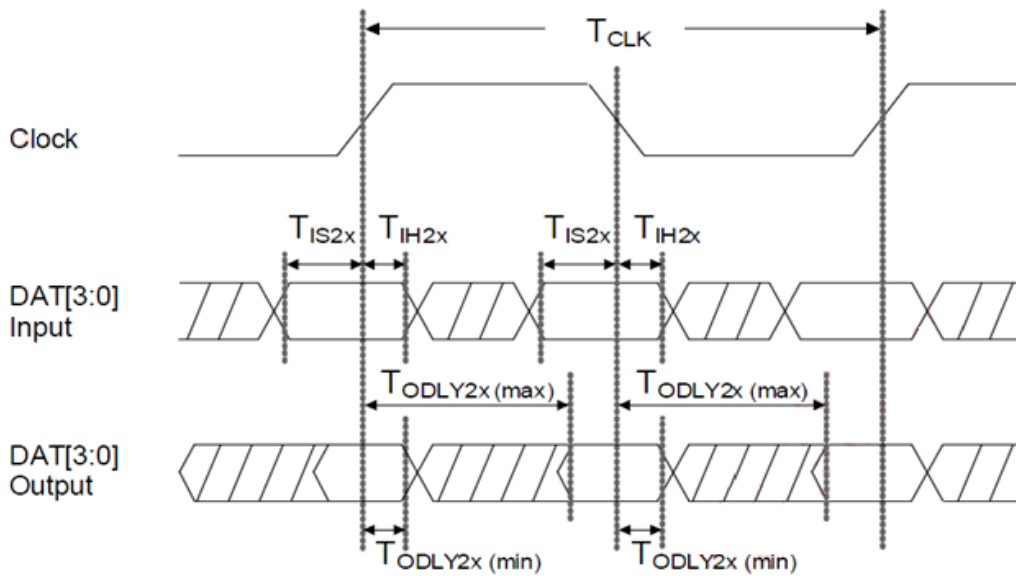
Table shows SDIO Timing Data—SDR104 Mode (208MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{pp}$	CLK Frequency	SDR104	0	-	208	MHz
$T_{CLK}$	Clock Time	SDR104	4.8	-	-	ns
$T_{IS}$	Input Setup Time	SDR104	1.4	-	-	ns
$T_{IH}$	Input Hold Time	SDR104	0.8	-	-	ns
$T_{CR}, T_{CF}$	Rise time, fall time $T_{CR}, T_{CF} < 0.96\text{ns}(\text{max})$ at 208MHz $C_{CARD}=10\text{pF}$	SDR104	-	-	$0.2 \cdot T_{CLK}$	ns
$T_{OP}$	Card output phase	SDR104	0	-	10	ns
$T_{ODW}$	Output timing of variable data window	SDR104	2.88	-	-	ns

### 3.4.2.4 DDR50 Mode (50MHz) (1.8V)



SDIO CMD Timing Diagram - DDR50 Mode (50 MHz)



SDIO DAT[3:0] Timing Diagram - DDR50 Mode<sup>1</sup> (50 MHz)

<sup>1</sup> In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

Symbol	Parameter	Condition	Min	Typ	Max	Units
<b>Clock</b>						
T <sub>CLK</sub>	Clock time	DDR50	20	-	-	ns
T <sub>CR</sub> , T <sub>CF</sub>	Rise time, fall time	DDR50	-	-	0.2*T <sub>CLK</sub>	Ns
Clock Duty		DDR50	45	-	55	%
<b>CMD Input</b>						
T <sub>IS</sub>	Input setup time	DDR50	6	-	-	ns
T <sub>IH</sub>	Input hold time	DDR50	0.8	-	-	ns
<b>CMD Output</b>						
T <sub>ODLY</sub>	Output delay time during data transfer mode	DDR50	-	-	13.7	ns
T <sub>OHLd</sub>	Output hold time	DDR50	1.5	-	-	ns
<b>DAT [3:0] Input</b>						
T <sub>IS2X</sub>	Input setup time	DDR50	3	-	-	ns
T <sub>IH2X</sub>	Input hold time	DDR50	0.8	-	-	ns
<b>DAT [3:0] Output</b>						
T <sub>ODLY2X(max)</sub>	Output delay time during data transfer mode	DDR50	-	-	7	ns
T <sub>ODLY2X(min)</sub>	Output hold time	DDR50	1.5	-	-	ns

SDIO Timing Data - DDR50 Mode (50MHz)

### 3.4.3 PCI Express Interface

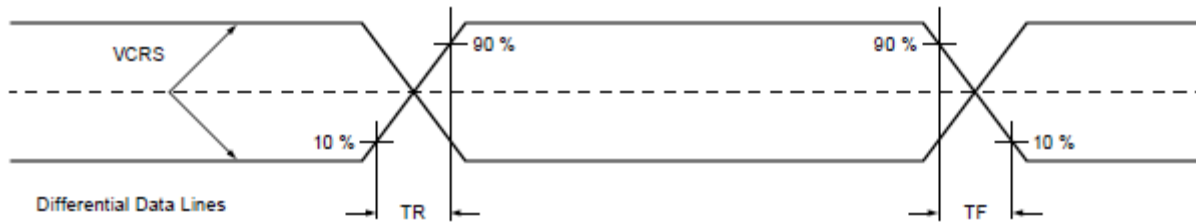
#### 3.4.3.1 Differential Tx Output Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps $\pm$ 300 PPM. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
$V_{Tx\_DIFFpp}$	Differential peak-to-peak output voltage $V_{Tx\_DIFFpp} = 2 *  V_{Tx\_D+} - V_{Tx\_D-} $	0.800	--	1.2	V
$V_{Tx\_DE\_RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	db
$T_{Rx\_EYE}$	Minimum Tx eye width	0.75	--	--	UI
$T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$	Maximum time between jitter median and maximum deviation from median	--	--	0.125	UI
$T_{Tx\_RISE}$ , $T_{Tx\_FALL}$	D+/D- Tx output rise/fall time	0.125	--	--	UI
$V_{Tx\_CM\_DC\_ACTIVE\_IDLE\_DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0-	-	100	mV
$V_{Tx\_CM\_DC\_LINE\_DELTA}$	Absolute delta of DC common mode voltage between D+ and D-	0-	-	25	mV
$V_{Tx\_IDLE\_DIFFp}$	Electrical idle differential peak output voltage	0	--	20	mV
$V_{Tx\_RCV\_DETECT}$	Voltage change allowed during receiver detection	--	--	600	mV
$V_{Tx\_DC\_CM}$	Tx DC common mode voltage	--	--	3.6	V
$I_{Tx\_SHORT}$	Tx short circuit current limit	--	--	90	mA
$T_{Tx\_IDLE\_MIN}$	Minimum time spent in electrical idle	50	--	--	UI
$T_{Tx\_IDLE\_SET\_TO\_IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	--	--	20	UI
$T_{Tx\_IDLE\_TO\_DIFF\_DATA}$	Maximum time to transition to valid Tx specifications after leaving an electrical idle condition	--	--	20	UI
$RL_{Tx\_DIFF}$	Differential return loss	10	--	--	dB
$RL_{Tx\_CM}$	Common mode return loss	6	--	--	dB
$C_{Tx}$	AC coupling capacitor	75	--	200	nF
$T_{Crosstalk}$	Crosstalk random timeout	0	--	1	ms

### 3.4.3.2 Differential Rx Input Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps $\pm$ 300 ppm. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
V <sub>Rx_DIFFpp</sub>	Differential peak-to-peak voltage $V_{Rx\_DIFFpp} = 2 *  V_{Rx\_D+} - V_{Rx\_D-} $	0.175	--	1.2	V
T <sub>Rx_EYE</sub>	Minimum receiver eye width	0.4	--	--	UI
T <sub>Rx_EYE_MEDIAN_MAX_JIT</sub>	Maximum time between jitter median and maximum deviation from median	--	--	0.3	UI
V <sub>Rx_CM_ACp</sub>	AC peak common mode input voltage	--	--	150	mV
RL <sub>Rx_DIFF</sub>	Differential return loss	10	--	--	dB
RL <sub>Rx_CM</sub>	Common mode return loss	6	--	--	dB
Z <sub>Rx_DIFF_DC</sub>	DC differential input impedance	80	100	120	$\Omega$
Z <sub>Rx_DC</sub>	DC input impedance	40	50	60	$\Omega$
Z <sub>Rx_HIGH_IMP_DC_POS</sub>	Powered down DC input impedance positive	50	--	--	k
Z <sub>Rx_HIGH_IMP_DC_NEG</sub>	Powered down DC input impedance negative	1	--	--	k $\Omega$
V <sub>Rx_IDLE_DET_DIFFpp</sub>	Electrical idle detect threshold	65	--	175	mV
T <sub>Rx_IDLE_DET_DIFF_ENTERTIME</sub>	Unexpected electrical idle enter detect threshold integration time	--	--	10	ms
L <sub>Rx_SKEW</sub>	Total skew	---	-2	0	ns

### 3.4.4 USB Interface



#### 3.4.4.1 USB LS Driver and Receiver Parameters

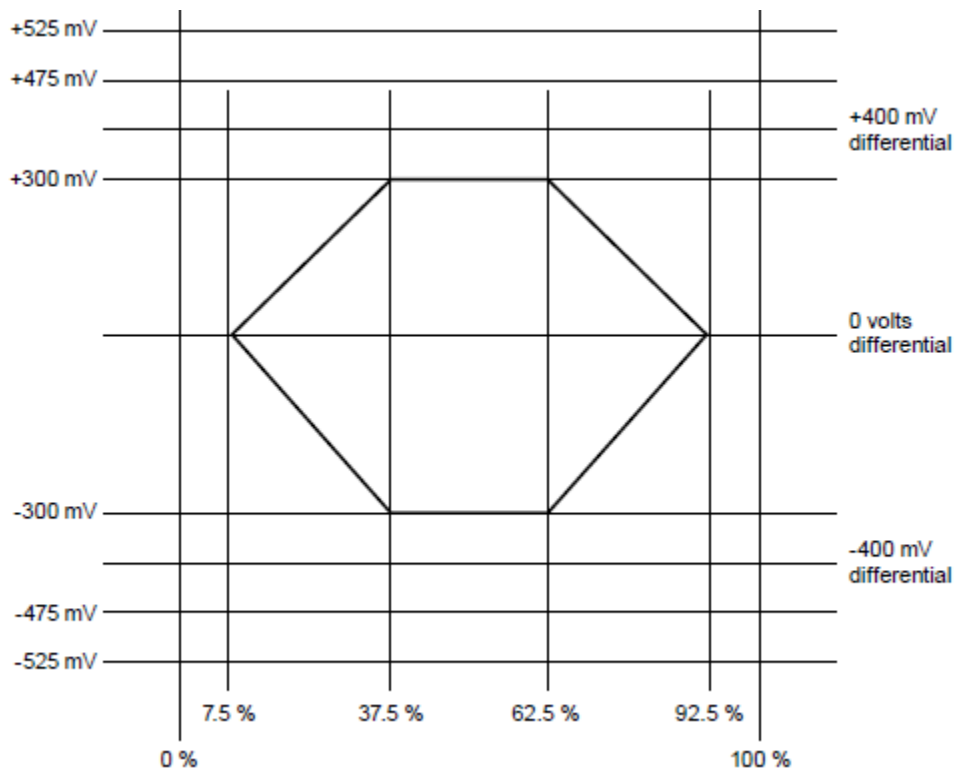
Symbol	Parameter	Min	Typ	Max	Units
BR	Baud rate	-	1.5	-	Mbps
BR <sub>ppm</sub>	Baud rate tolerance	-15000	-	15000	ppm
<b>Driver specifications</b>					
V <sub>OH</sub>	Output single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V.	2.8	-	3.6	V
V <sub>OL</sub>	Output single ended low Defined with 1.425 kΩ pull-down resistor to ground.	0	-	0.3	V
V <sub>CRS</sub>	Output single crossover voltage	1.3	-	2.0	V
T <sub>LR</sub>	Data rise time • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75	-	300	ns
T <sub>LF</sub>	Data fall time • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75	-	300	ns
T <sub>LRFM</sub>	Rise and fall time matching	80	-	125	%
T <sub>UDJ1</sub>	Source jitter total: to next transition • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-95	-	95	ns
T <sub>UDJ2</sub>	Source jitter total: for paired transitions • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-150	-	150	ns
<b>Receiver specifications</b>					
V <sub>IH</sub>	Input single ended high	2.0	-	-	V
V <sub>IL</sub>	Input single ended low	-	-	0.8	V
V <sub>DI</sub>	Differential input sensitivity	0.2	-	-	V

### 3.4.4.2 USB FS Driver and Receiver Parameters

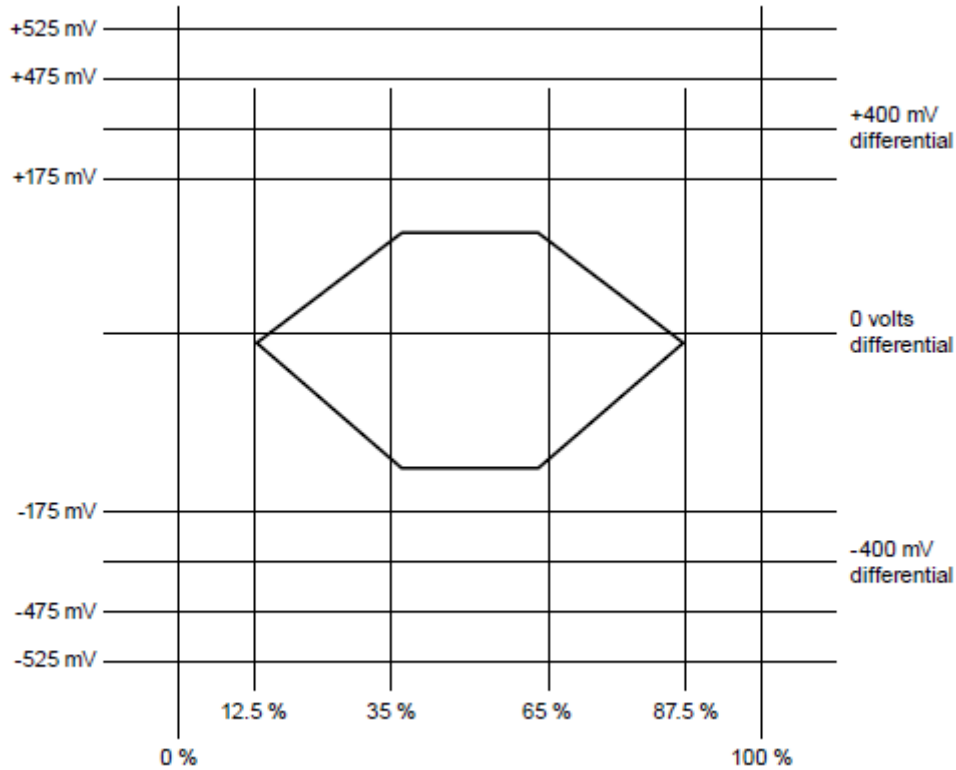
Symbol	Parameter	Min	Typ	Max	Units
BR	Baud rate	-	12	-	Mbps
BR <sub>ppm</sub>	Baud rate tolerance	-2500	-	2500	ppm
<b>Driver specifications</b>					
V <sub>OH</sub>	Output single ended high Defined with 1.425 k $\Omega$ pull-up resistor to 3.6V.	2.8	-	3.6	V
V <sub>OL</sub>	Output single ended low Defined with 1.425 k $\Omega$ pull-down resistor to ground.	0	-	0.3	V
V <sub>CRS</sub>	Output single crossover voltage	1.3	-	2.0	V
T <sub>FF</sub>	Data fall time • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4	-	20	ns
T <sub>FR</sub>	Data rise time • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4	-	20	ns
T <sub>DJ1</sub>	Source jitter total: to next transition • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-3.5	-	3.5	ns
T <sub>DJ2</sub>	Source jitter total: for paired transitions • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-4	-	4	ns
T <sub>FDEOP</sub>	Source jitter for differential transition to SE0 transition Defined at crossover point of differential data signals.	-2	-	5	ns
<b>Receiver specifications</b>					
V <sub>IH</sub>	Input single ended high	2.0	-	-	V
V <sub>IL</sub>	Input single ended low	-	-	0.8	V
V <sub>DI</sub>	Differential input sensitivity	0.2	-	-	V
T <sub>JR1</sub>	Receiver jitter: to next transition Defined at crossover point of differential data signals.	-18.5	-	18.5	ns
T <sub>JR2</sub>	Receiver jitter: for paired transitions Defined at crossover point of differential data signals.	-9	-	9	ns

### 3.4.4.3 USB HS Driver and Receiver Parameters

Symbol	Parameter	Min	Typ	Max	Units
BR	Baud rate	-	480	-	Mbps
BR <sub>ppm</sub>	Baud rate tolerance	-500	-	500	ppm
<b>Driver specifications</b>					
V <sub>HSOH</sub>	Data signaling high	360	-	440	mV
V <sub>HSOL</sub>	Data signaling low	-10	-	10	mV
T <sub>HSR</sub>	Data rise time • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	500	-	-	ns
T <sub>HSF</sub>	Data fall time • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-500	-	-	ns
--	Source jitter See below figure	-	-	-	-
<b>Receiver specifications</b>					
--	Differential input signaling levels See below figure	-	-	-	-
V <sub>HSCM</sub>	Input single ended low	-50	-	500	mV
--	Receiver jitter tolerance See below figure	-	-	-	-



USB HS Tx Eye Diagram Pattern Template Diagram



USB HS Rx Eye Diagram Pattern Template Diagram

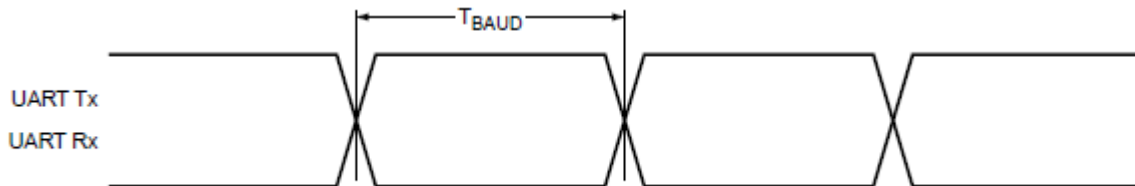
### 3.4.4.4 USB SS Gen 1 Driver and Receiver Parameters

Symbol	Parameter	Min	Typ	Max	Units
<b>Driver specifications</b>					
$V_{O-DIFF-PP}$	Output differential peak-peak voltage swing	0.8	-	1.2	V
$V_{O-DIFF-PP-LOW}$	Output differential peak-peak voltage swing, low power There is node-emphasis requirement in this mode. De-emphasis is implementation specific for this mode	0.4	-	1.2	V
$V_{O-AC-CM-ACTIVE-PP}$	Output AC common mode voltage active peak-peak	-	-	100	mV
$V_{O-EMPH}$	Output emphasis	3	-	4	dB
$R_{O-DC-DIFF}$	Output DC differential impedance	72	-	120	$\Omega$
$R_{O-DC-CM}$	Output DC common mode impedance Defined with respect AC ground over a voltage of 0-500mV	18	-	30	$\Omega$
$T_{O-CDR\_SLEW}$	Output Frequency slew rate This value includes all SSC and jitter sources. See the USB 3.0 Specification.	-	-	10	Ms/s
$J_{O-DJ-DO}$	Output jitter, deterministic, delta-delta	-	-	0.205	UI

	Driver jitter does not include correlated bounded jitter created by the driver emphasis				
<b>Receiver specifications</b>					
V <sub>IDPPS</sub>	Input differential sensitivity <ul style="list-style-type: none"> <li>Refer to the initial eye opening</li> <li>Defined after applying reference receiver CTLE function</li> </ul> See the USB 3.0 Specification.	30	-	-	mV
V <sub>IN-LFPS-DET-PP</sub>	Input Low Frequency Periodic Signaling defect threshold, peak-peak.	100	-	300	mV
R <sub>IN-DC-DIFF</sub>	Input DC differential impedance	72	-	120	Ω
R <sub>IN-DC-CM</sub>	Input DC common mode impedance	18	-	30	Ω
V <sub>Tx-RCV-DETECT</sub>	Voltage change allowed during detection Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an “off” receiver’s input goes below ground	-	-	600	mV

### 3.4.5.High-Speed UART Interface

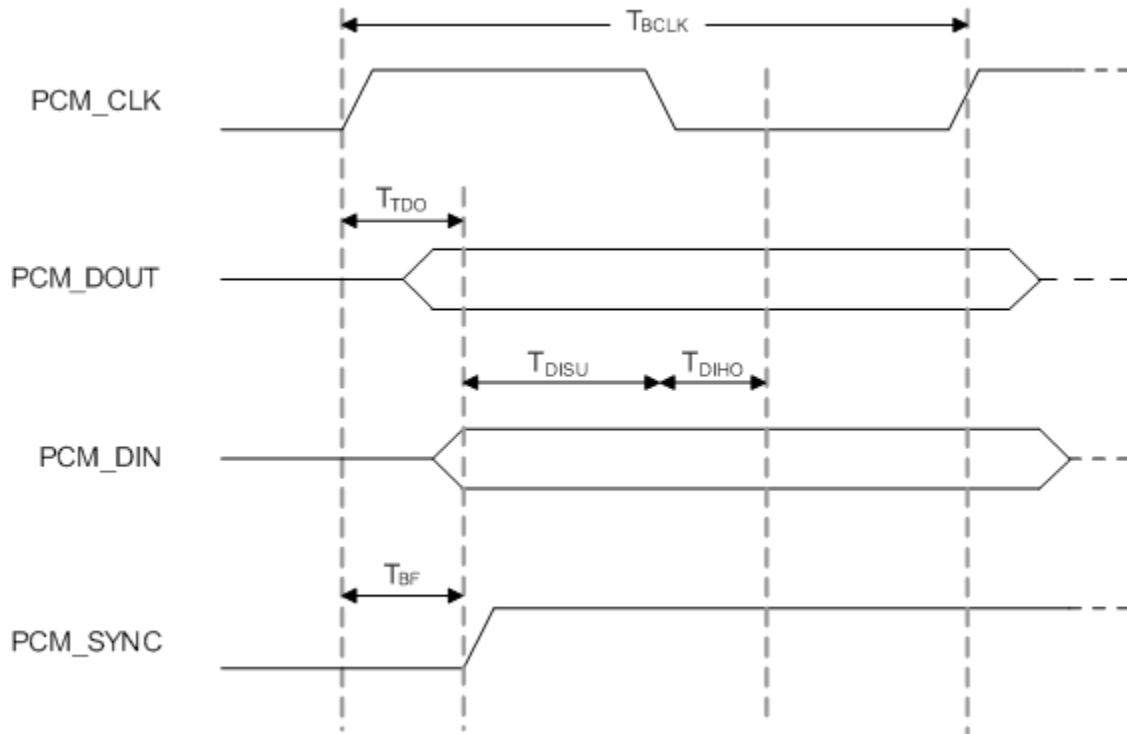
The AW-XM369 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Typ	Max	Units
T <sub>BAUD</sub>	Baud rate	26MHz input clock	250	-	-	ns

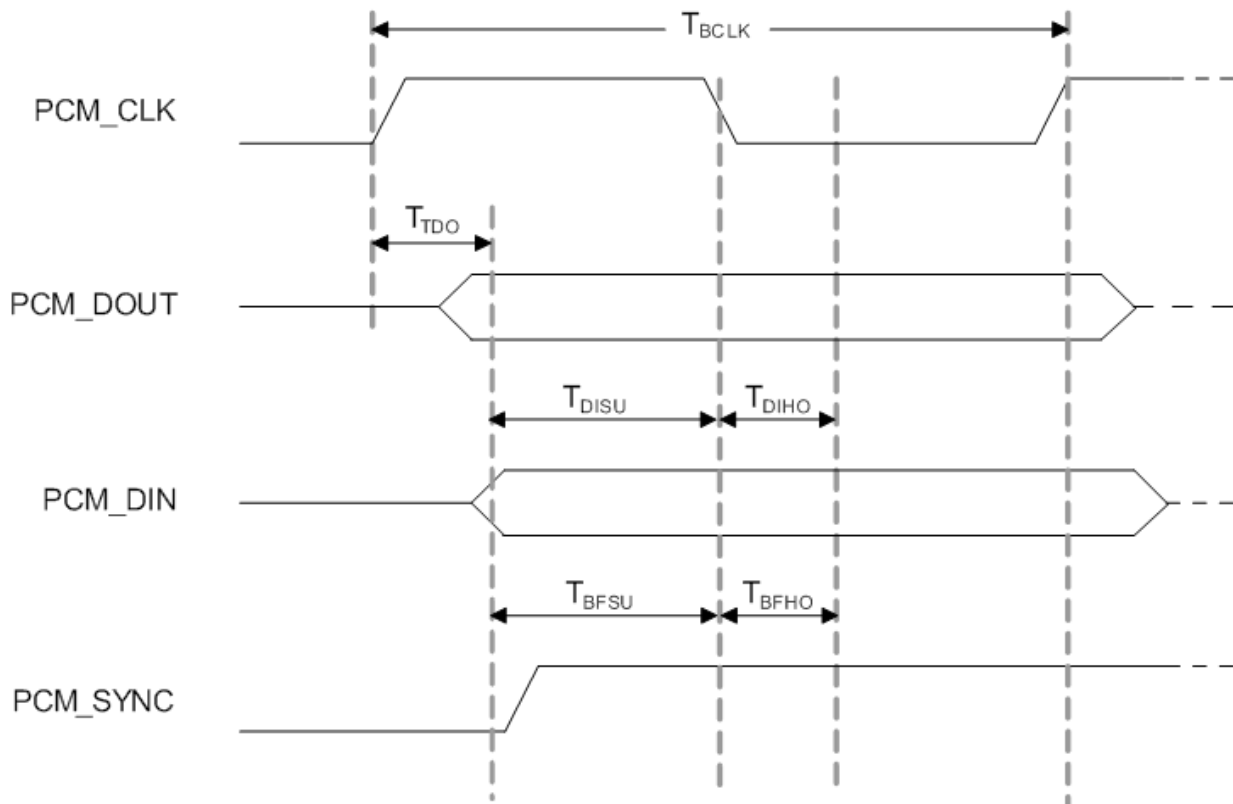
### 3.4.6 PCM Interface

#### 3.4.6.1 PCM Timing Specification – Master Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
$F_{BCLK}$	--	--	--	2/2.048	--	MHz
Duty Cycle $_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK}$ rise/fall	--	--	--	3	--	ns
$T_{DO}$	--	--	--	--	15	ns
$T_{DISU}$	--	--	20	--	--	ns
$T_{DIHO}$	--	--	15	--	--	ns
$T_{BF}$	--	--	--	--	15	ns

### 3.4.6.2 PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
$F_{BCLK}$	--	--	--	2/2.048	--	MHz
Duty Cycle $_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK}$ rise/fall	--	--	--	3	--	ns
$T_{DO}$	--	--	--	--	30	ns
$T_{DISU}$	--	--	15	--	--	ns
$T_{DIHO}$	--	--	10	--	--	ns
$T_{BFSU}$	--	--	15	--	--	ns
$T_{BFHO}$	--	--	10	--	--	ns

### 3.5 Timing Sequence

AW-XM369 power up timing sequence.

TBD

## **3.6 Power Consumption\***

### **3.6.1 WLAN**

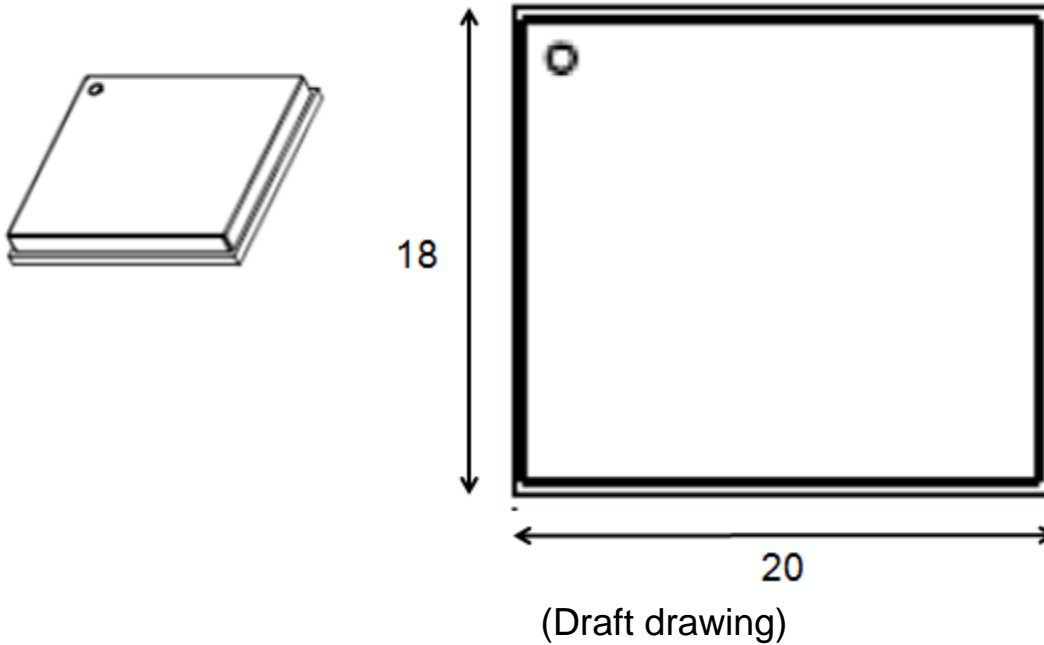
TBD

### **3.6.2 Bluetooth**

TBD

## 4. Mechanical Information

### 4.1 Mechanical Drawing



## 5. Packing Information

TBD