正基科技股份有限公司

SPECIFICATION

SPEC. NO.： ____________ **REV：** 1.3

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PRODUCT NAME： AP6201

Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW		APPROVED	DCC ISSUE
	PM	QA		

AMPAK

AP6201

WiFi 11b/g/n + Bluetooth V5.0
Module Spec Sheet

Revision History

Date	Revision Content	Revised By	Version
2017/07/26	- Draft Spec	Richard	0.1
2017/08/22	- Update Spec	Eason	1.0
2017/09/21	- Update Pin assignment	Eason	1.1
2018/03/05	- Update BT Spec	Richard	1.2
2018/08/28	- Modify Wi-Fi Spec	Richard	1.3

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1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the Wi-Fi, Bluetooth functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

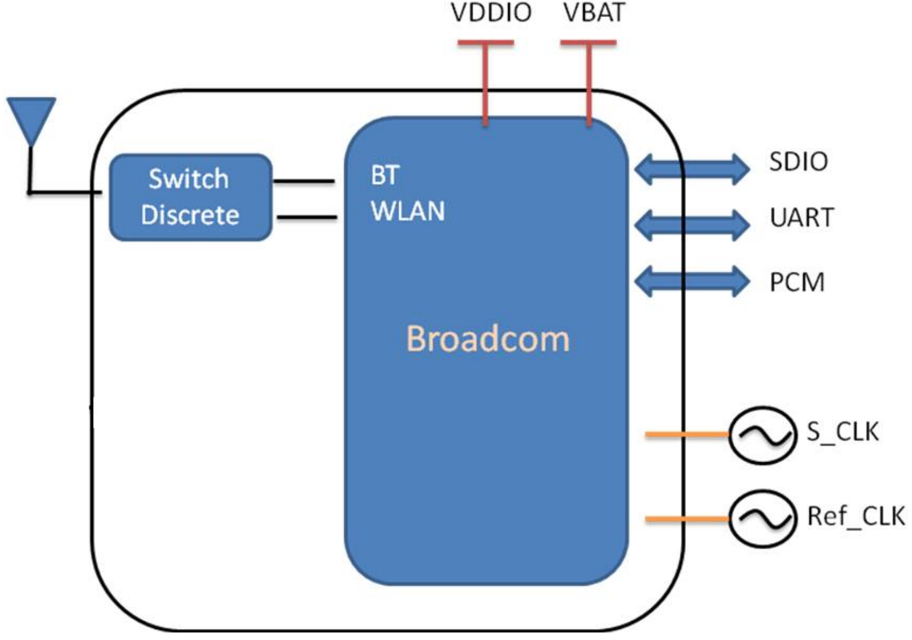
The wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72Mbps with single stream in 802.11n to connect to the wireless LAN. The integrated module provides SDIO interface for Wi-Fi, UART / PCM interface for Bluetooth.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

2. Features

- IEEE 802.11b/g/n single-band radio with virtual-simultaneous single-band operation
- Single-stream spatial multiplexing up to 72 Mbps data rate.
- Supports Bluetooth V5.0+EDR with integrated PA for Class 1.5 and Low Energy (BLE).
- Concurrent Bluetooth, and WLAN operation
- Simultaneous BT/WLAN receive with single antenna
- Supports standard SDIO v3.0 and backward compatible with SDIO v2.0 host interfaces.
  - SDIO v3.0(4-bit) — up to 80 MHz clock rate in SDR50 mode, 40MHz clock rate in 40MHz.
- BT host digital interface:
  - UART (up to 4 Mbps)
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

A simplified block diagram of the module is depicted in the figure below.



3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

4. General Specification

4.1 General Specification

Model Name	AP6201
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 12 x 12 x 1.5 (typical) mm
WiFi Interface	SDIO v2.0/v3.0
BT Interface	UART / PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 105°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Optimal RF performance specified in the data sheet, however, is guaranteed only for -20~75 ℃

The AP6201 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.2V < VBAT < 3.8V.

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5.25	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	2.07	V

4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	deg.C
VBAT	3.0	3.3	3.8	V
VDDIO	1.62	1.8	1.98	V

5. Wi-Fi RF Specification

5.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature	Description	
WLAN Standard	IEEE 802.11b/g/n/ac, WiFi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch13	
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11g/n : 64-QAM,16-QAM, QPSK, BPSK 802.11ac : 256-QAM, 64-QAM,16-QAM, QPSK, BPSK	
Output Power	802.11b /CCK	: 16.5 dBm ± 1.5 dB @ EVM ≤ -9dB
	802.11g /64-QAM(R=3/4)	: 15.5 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11n /64-QAM(R=5/6)	: 14.5 dBm ± 1.5 dB @ EVM ≤ -27dB
Receive Sensitivity (11b) @8% PER	- 1Mbps	PER @ -96 dBm, ± 2dB
	- 2Mbps	PER @ -90 dBm, ± 2dB
	- 5.5Mbps	PER @ -89 dBm, ± 2dB
	- 11Mbps	PER @ -88 dBm, ± 2dB
Receive Sensitivity (11g) @10% PER	- 6Mbps	PER @ -90 dBm, ± 2dB
	- 9Mbps	PER @ -88 dBm, ± 2dB
	- 12Mbps	PER @ -87 dBm, ± 2dB
	- 18Mbps	PER @ -85 dBm, ± 2dB
	- 24Mbps	PER @ -83 dBm, ± 2dB
	- 36Mbps	PER @ -80 dBm, ± 2dB
	- 48Mbps	PER @ -78 dBm, ± 2dB
	- 54Mbps	PER @ -76 dBm, ± 2dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -89 dBm, ± 2dB
	- MCS=1	PER @ -85 dBm, ± 2dB
	- MCS=2	PER @ -84 dBm, ± 2dB
	- MCS=3	PER @ -82 dBm, ± 2dB
	- MCS=4	PER @ -80 dBm, ± 2dB
	- MCS=5	PER @ -78 dBm, ± 2dB
	- MCS=6	PER @ -76 dBm, ± 2dB
	- MCS=7	PER @ -74 dBm, ± 2dB
Maximum Input Level	802.11b : -10dBm	
	802.11g/n : -20dBm	

Antenna Reference	Small antennas with 0~2 dBi peak gain

6. Bluetooth Specification

6.1 Bluetooth Specification

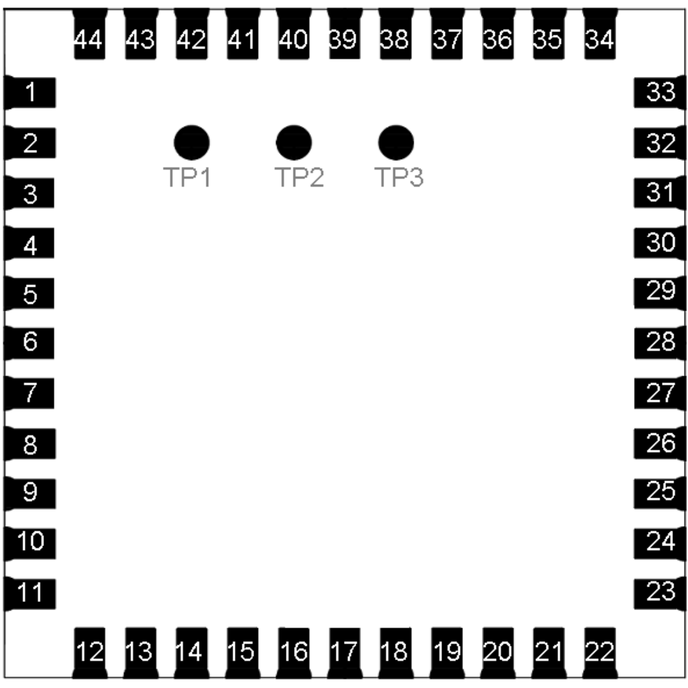
Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V5.0 & 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	FHSS, GFSK, DPSK, DQPSK		
RF Specification			
	Min.	**Typical.**	**Max.**
Output Power[1]		7	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-88 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-88 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-84 dBm	
Maximum Input Level	GFSK (1Mbps) :-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

NOTE[1]：Output power can be configured by HCD firmware.

7. Pin Assignments

7.1 Pin Outline



7.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	NC	—	Floating (Don't connected to ground)
5	BT_GPIO_4	—	GPIO configuration pin
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	NC	—	Floating (Don't connected to ground)
9	VBAT	P	Main power voltage source input
10	XTAL_ON	I	Crystal Input
11	XTAL_OP	O	Crystal output
12	WL_REG_ON	I	Power up/down internal regulators used by WiFi section
13	WL_HOST_WAKE	O	WLAN to wake-up HOST

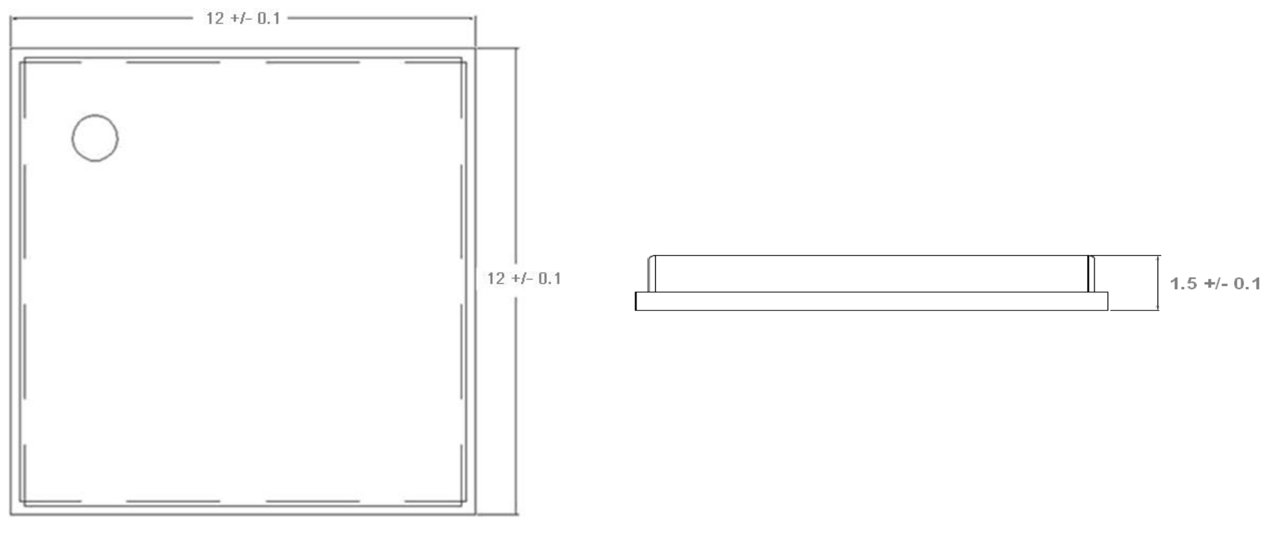
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	External Low Power Clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	BT_GPIO_3	I	GPIO configuration pin
30	BT_GPIO_5	I	GPIO configuration pin
31	GND	—	Ground connections
32	BT_GPIO_2	I	GPIO configuration pin
33	GND	—	Ground connections
34	BT_REG_ON	I	Power up/down internal regulators used by BT section
35	WLAN_UART_RXD	—	WLAN UART interface
36	GND	—	Ground connections
37	WLAN_DEV_WAKE	I/O	WLAN DEVICE WAKE UP
38	WLAN_UART_TXD	I/O	WLAN UART interface
39	WLAN_UART_CTS_IN	I/O	WLAN UART interface
40	WLAN_UART_RTS_OUT	I/O	WLAN UART interface
41	UART_RTS_N	O	Bluetooth UART interface
42	UART_TXD	O	Bluetooth UART interface
43	UART_RXD	I	Bluetooth UART interface
44	UART_CTS_N	I	Bluetooth UART interface
45	TP1(NC)	—	Floating (Don’t connected to ground)
46	TP2(NC)	—	Floating (Don’t connected to ground)
47	TP3(NC)	—	Floating (Don’t connected to ground)

8. Dimensions

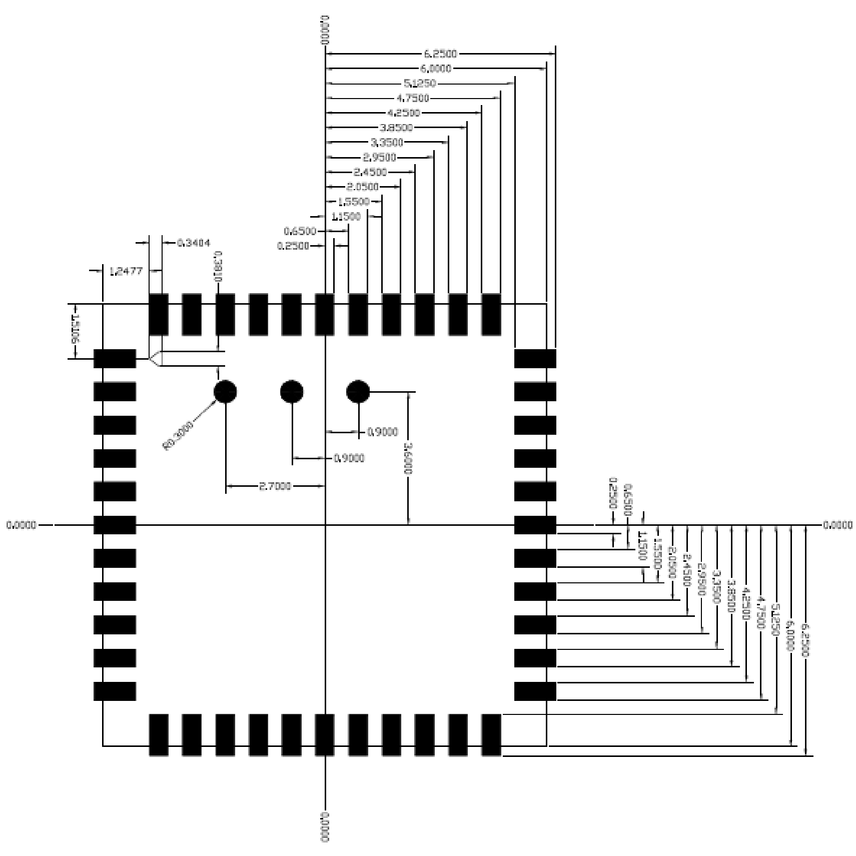
8.1 Physical Dimensions

(Unit: mm)

< TOP VIEW > < Side View >



< TOP VIEW >



8.2 Layout Recommendation

(Unit: mm)

< TOP VIEW >

9. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

10.1 SDIO Pin Description

All three package options of the WLAN section provide support for SDIO version 3.0 including the new UHS-I modes:

- DS: Default speed up to 25MHz (1.8V signaling), includeing 1- and 4-bit modes.
- HS: High speed up to 50MH (1.8V signaling).
- SDR12: SDR up to 25MHz (1.8V signaling).
- SDR25: SDR up to 50MHz (1.8V signaling).
- SDR50: SDR up to 80MHz (1.8V signaling).
- DDR50: DDR up to 40MHz (1.8V signaling).

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by SDIO interface. The ability to force control of gated clocks from within the device is also provided.

The following three functions are supported:

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 512B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

10. Host Interface Timing Diagram

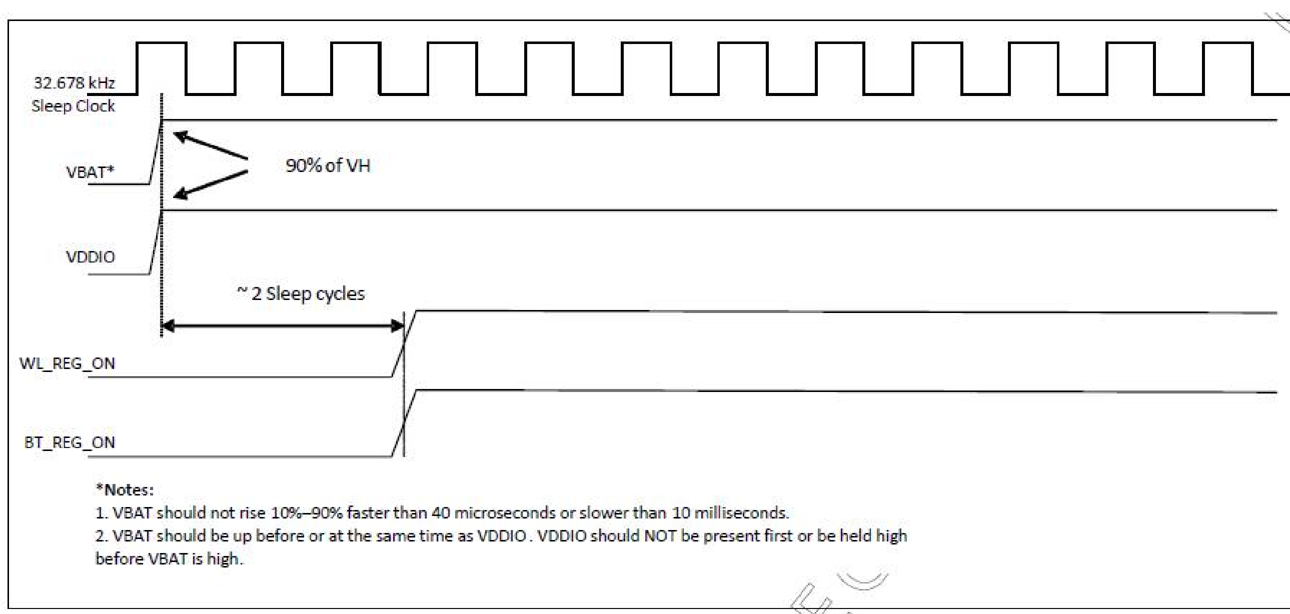
10.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

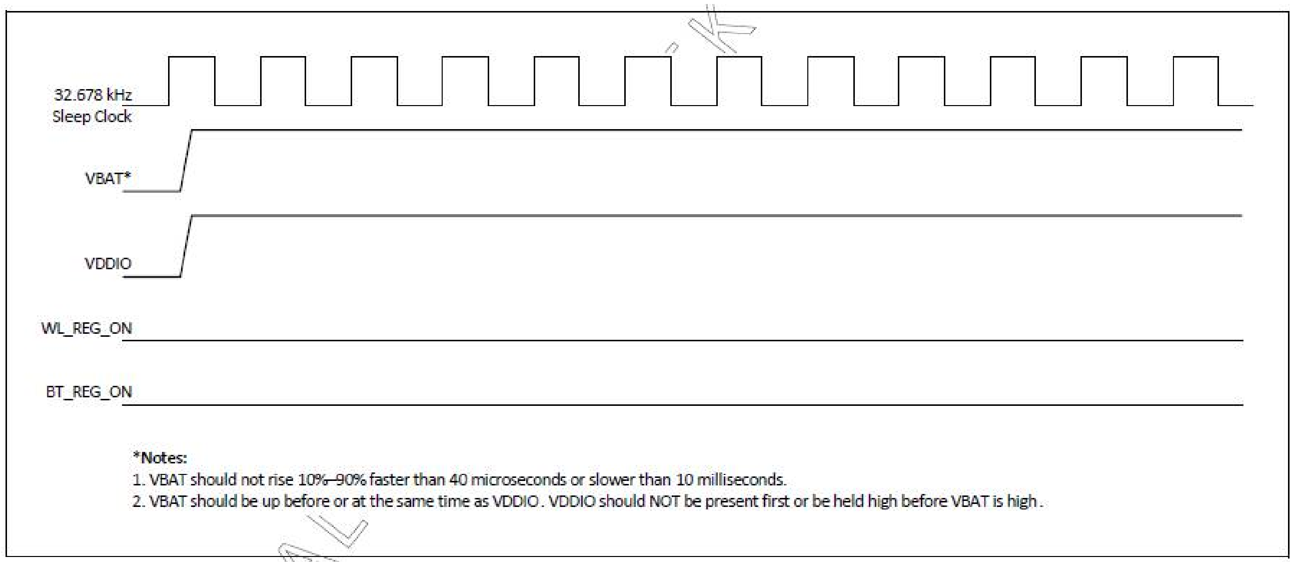
Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

※ WL_REG_ON: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.

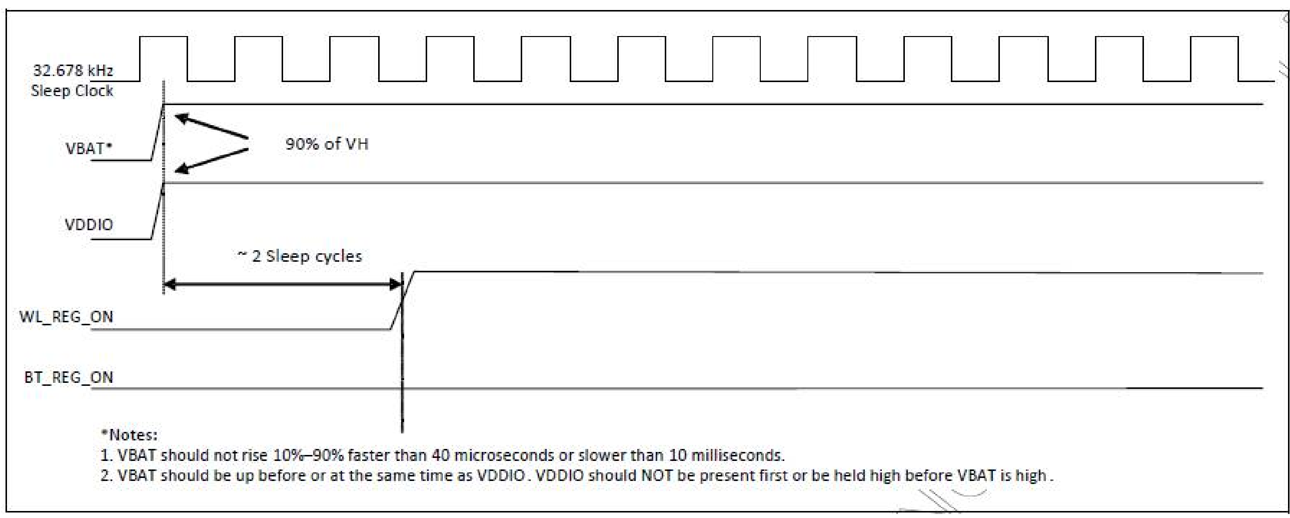
※ BT_REG_ON: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



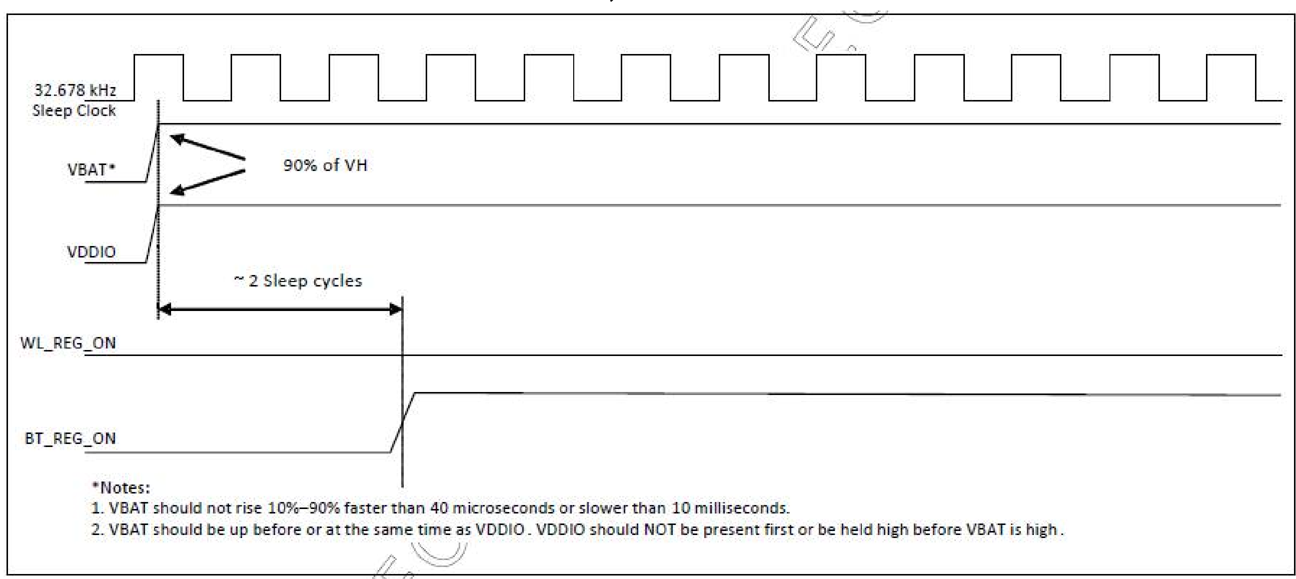
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

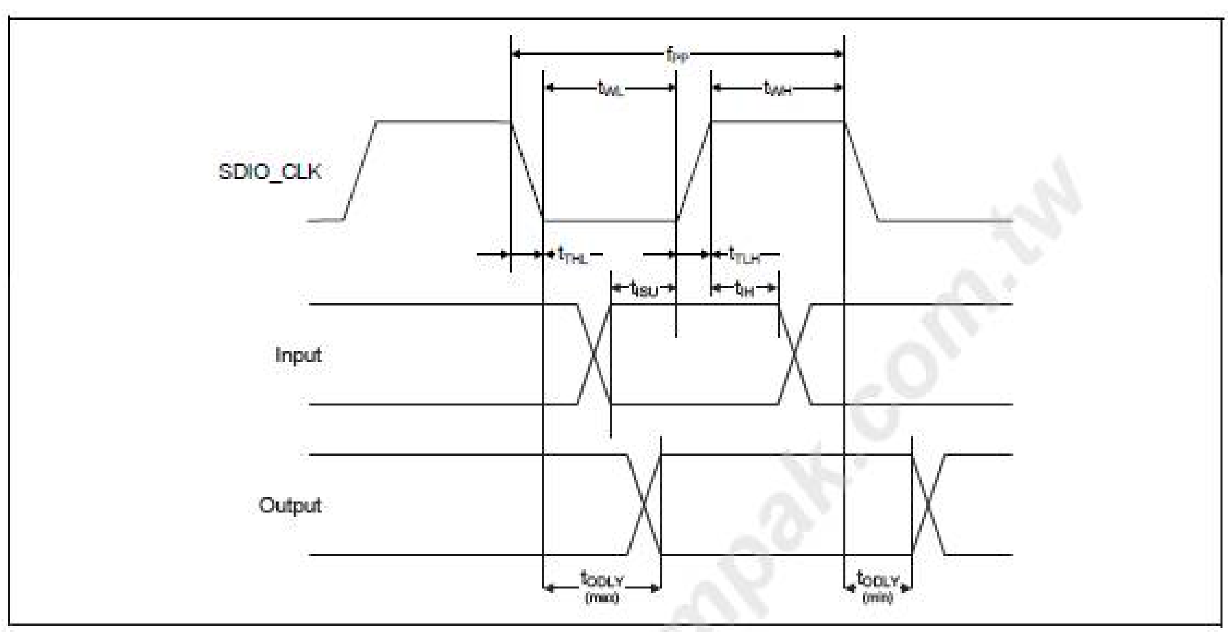


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

10.2 SDIO Default Mode Timing Diagram



SDIO Bus Timing[a] Parameters (Default Mode)

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. Min (Vih) = 0.7 × VDDIO and max. (Vil) = 0.2 × VDDIO.

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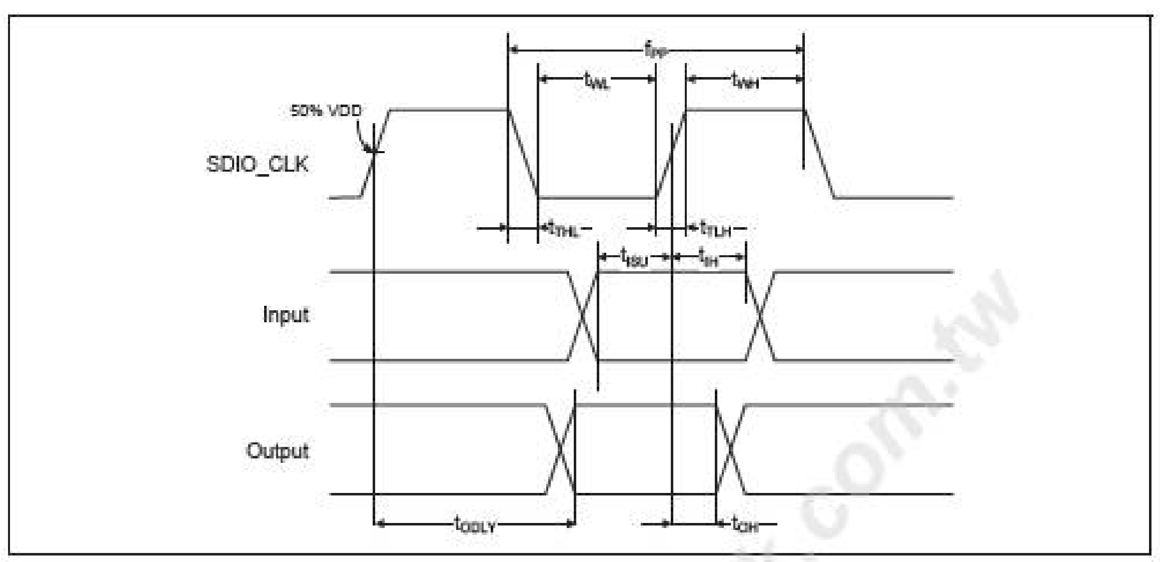
10.3 SDIO High Speed Mode Timing Diagram



SDIO Bus Timing[a] Parameters (High-Speed Mode)

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)	–	–	–	–	–
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)	–	–	–	–	–
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. Min (Vih) = 0.7 × VDDIO and max. (Vil) = 0.2 × VDDIO.

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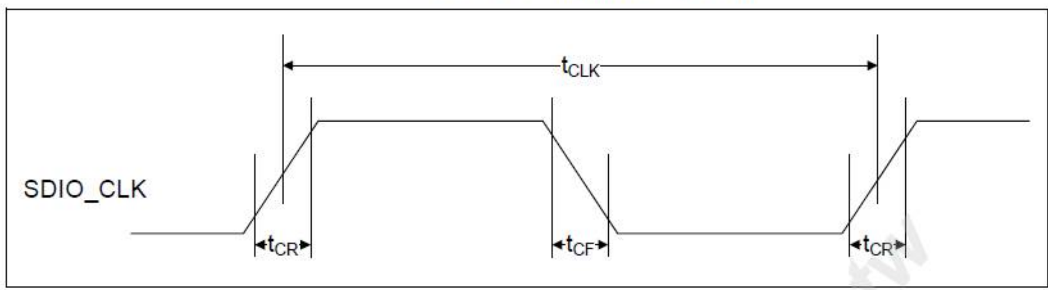
10.4 SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes)

SDIO Clock Timing (SDR Modes)

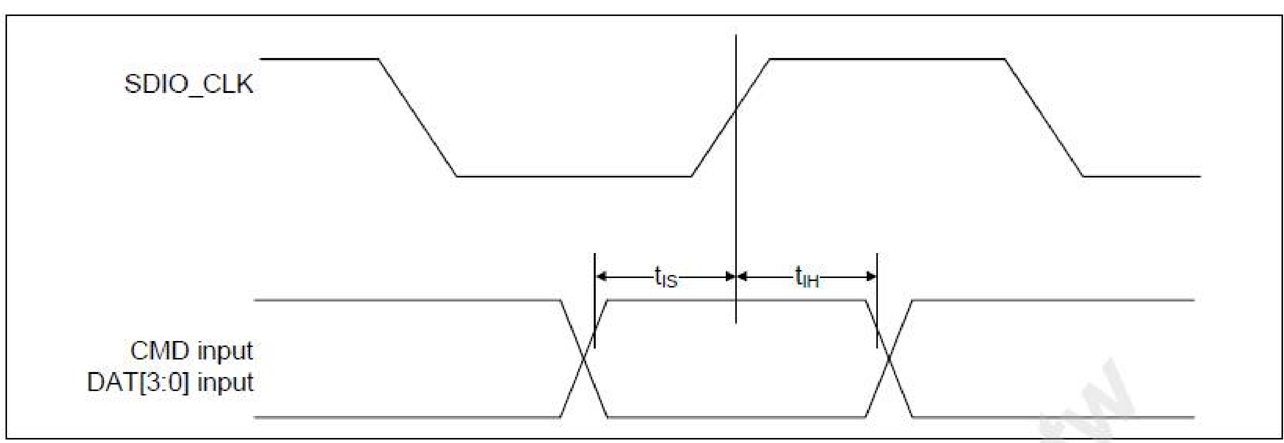


SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		12.5	–	ns	SDR50 mode
–	t_{CR}, t_{CF}	–	$0.2 \times t_{CLK}$	ns	t_{CR}, t_{CF} < 2.00 ns (max) @ 100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @ 208 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	30	70	%	–

Card Input timing (SDR Modes)

SDIO Bus Input Timing (SDR Modes)

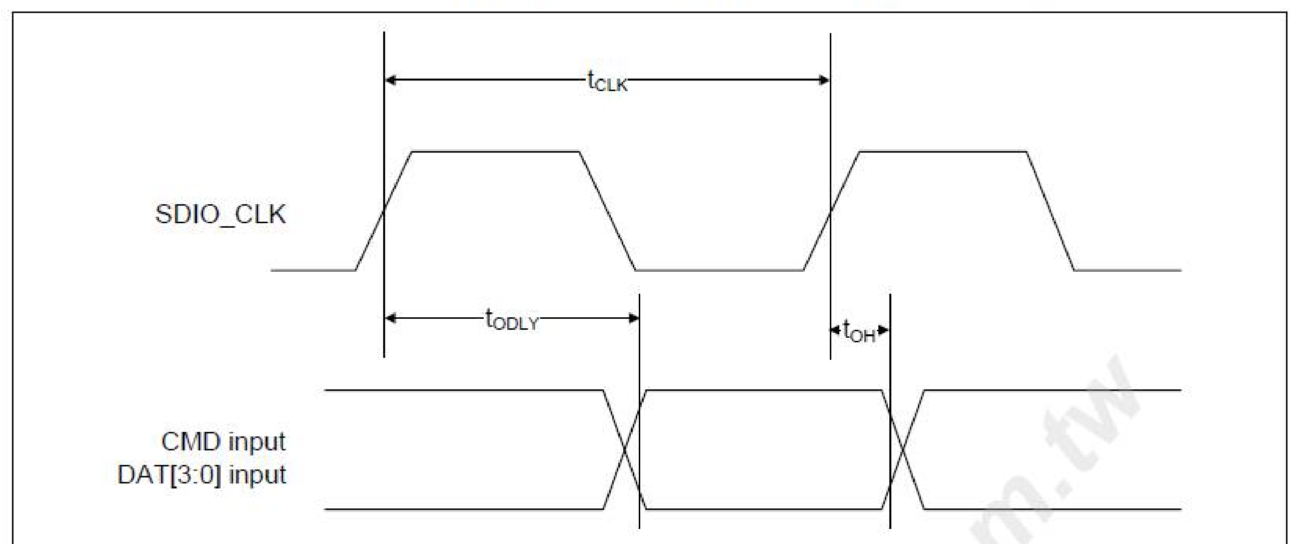


SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Minimum	Maximum	Unit	Comments
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

Card output timing (SDR Modes up to 80MHz)

SDIO Bus Output Timing (SDR Modes up to 80 MHz)

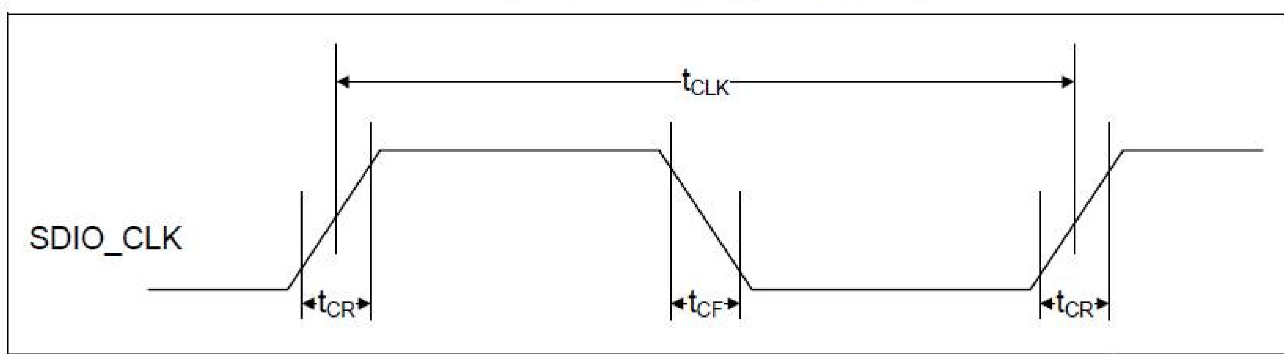


SDIO Bus Output Timing Parameters (SDR Modes up to 80 MHz)

Symbol	*Minimum*	*Maximum*	*Unit*	*Comments*
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

10.5 SDIO Bus Timing Specifications in DDR50 Mode

SDIO Clock Timing (DDR50 Mode)

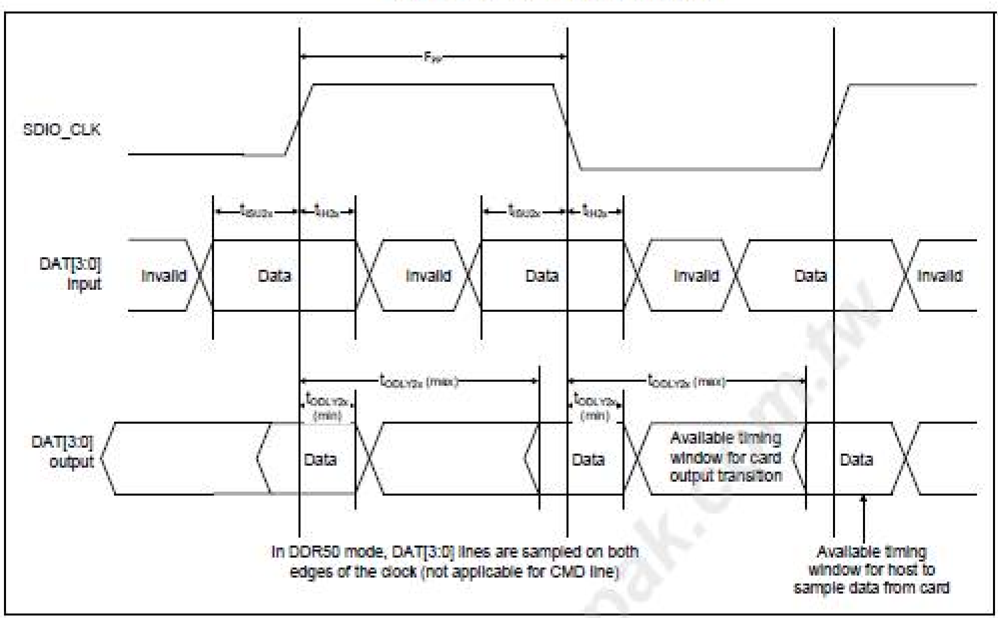


SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
–	t_{CLK}	25	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	45	55	%	–

Data Timing

SDIO Data Timing (DDR50 Mode)



SDIO Bus Timing Parameters (DDR50 Mode)

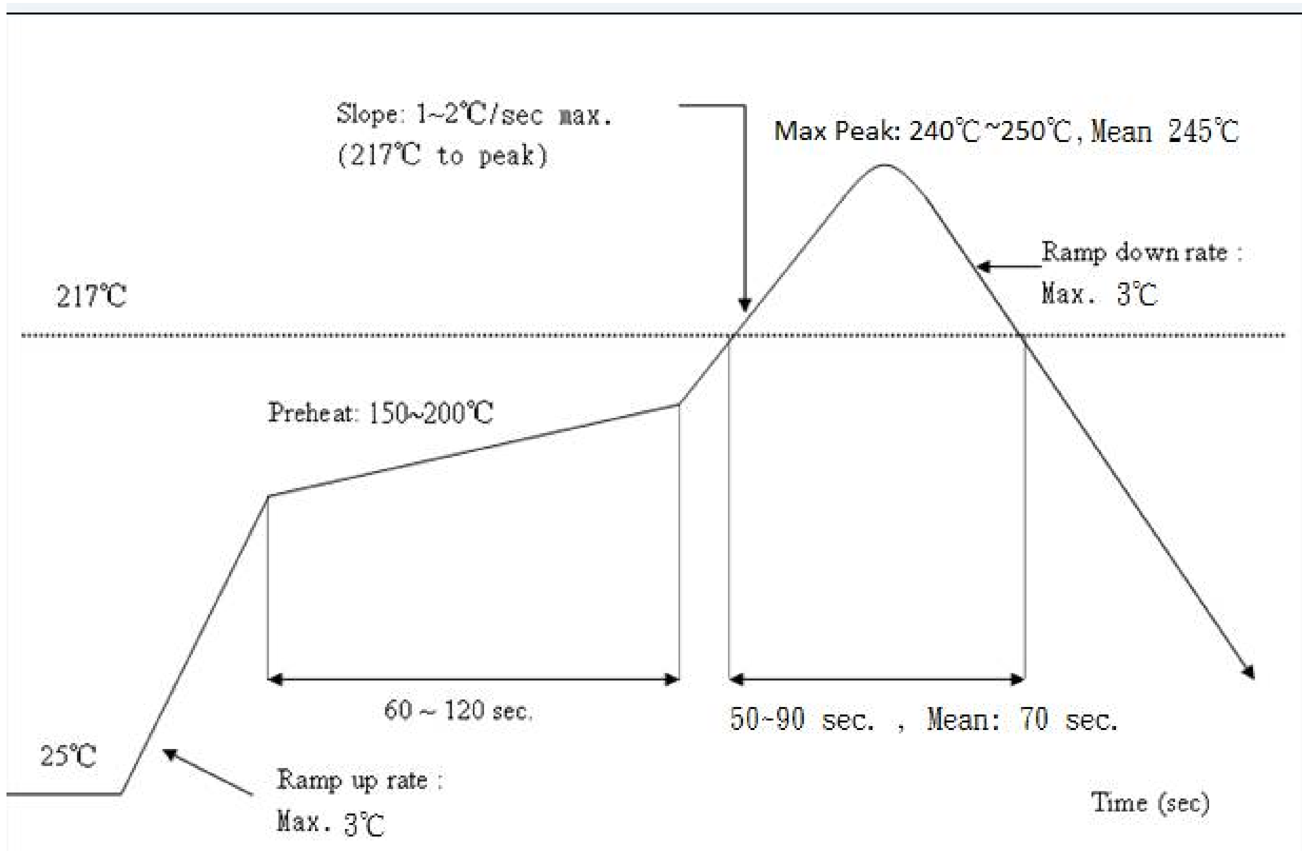
Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)

11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



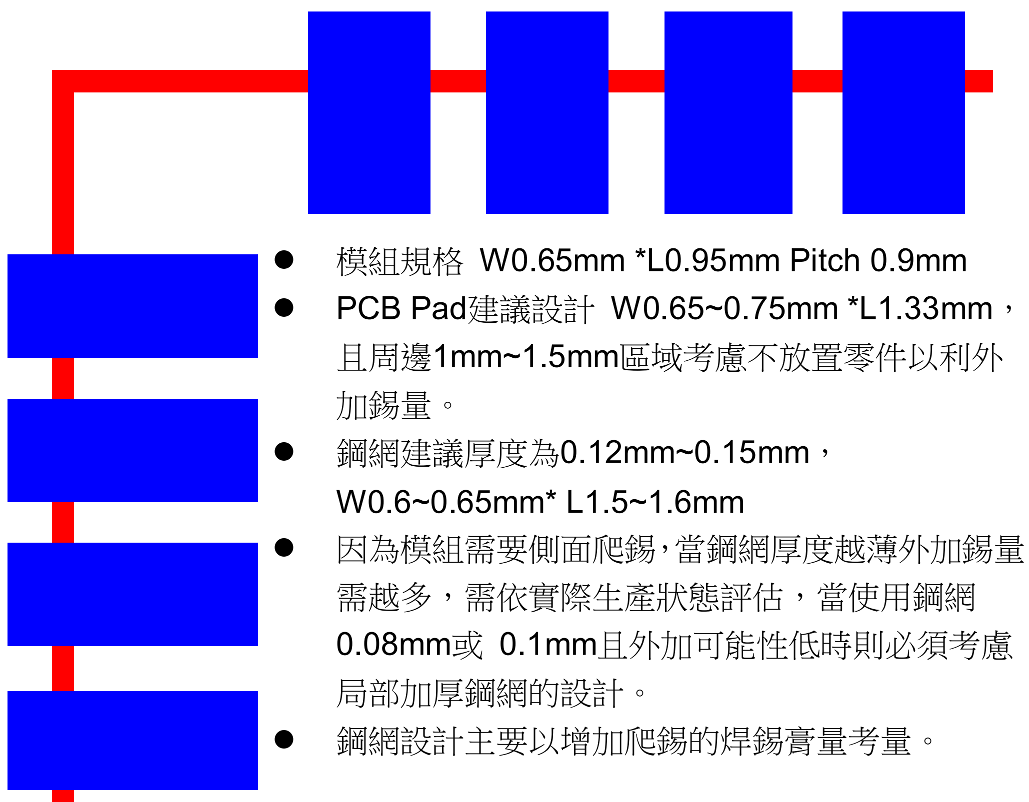
The notification of WiFi module before mounting:

The aperture of stencil should be larger than foot print of module, and the stencil thickness should be not less than 0.12mm.

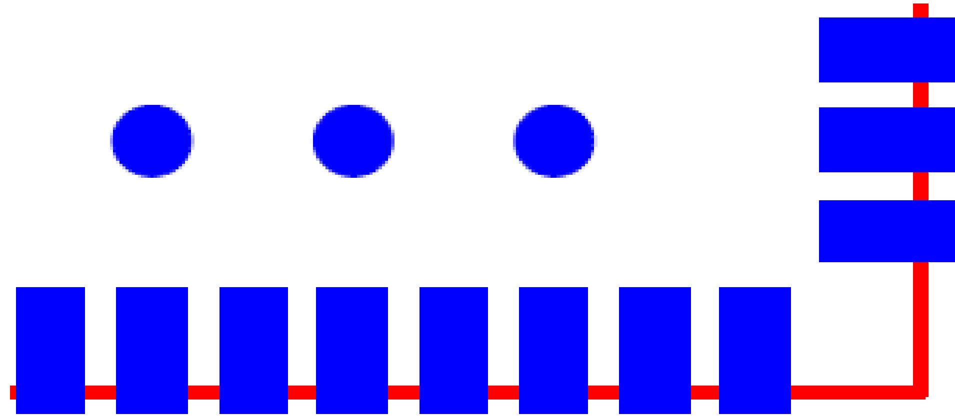
Reflow 時需使用 N2, 含氧量建議 5000 ppm 以下,

It must use N2 for reflow and suggest the concentration of oxygen less than 5000 ppm .

Solder Paste definition



- Module Specifications : W:0.65mm * L:0.95mm pitch 0.9 mm
- The proposed design W:0.65~0.75 mm * L:1.33mm. Consider not place other parts in the peripheral area of 1 mm ~ 1.5 mm to facilitate additional amount of solder for PCB pad.
- We Suggest the thickness of Stencil between 0.12 mm ~0.15mm, the W between 0.6~0.65mm and the L between L1.5~1.6mm.
- If the thickness of the stencil is thinner, we suggest to adding more solder, to increase the wetting ability. Depends on different production situation, if the stencil thickness is 0.08~0.1mm, and the module nearby area is no more space for expending soldering area, we will suggest to increase the stencil thickness to increase the wetting ability.
- The major consideration parts of stencil design is to increase the solder paste wetting ability.



模組規格 L 0.7mm
PCB Pad 設計 L 0.8mm
鋼網開孔建議 L0.5mm~0.6mm
適當內縮可以避免撐高造成高度影響

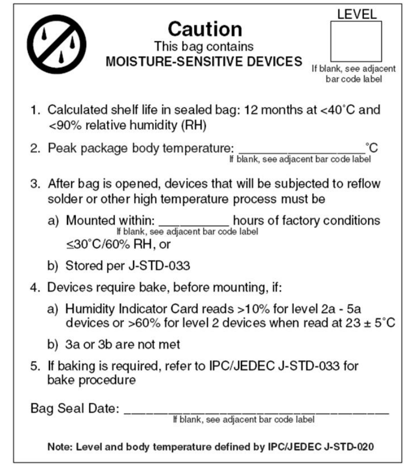
- Module Specifications L 0.7mm
- The design for PCB Pad : L:0.8mm
- We recommend the apertures for stencil L:0.5mm~0.6mm
- In order to avoid highness impact caused solder paste thickness, the stencil open size can be appropriately retracted

12. Package Information

12.1 Label

Label A→ Anti-static and humidity notice

Label B→ MSL caution / Storage Condition



Label C→ Inner box label .

PO:

AMK DEVICE: -

PKG S/N: 9PKGXXXXXXXXXXX

Model : AP6XXXX(HF)

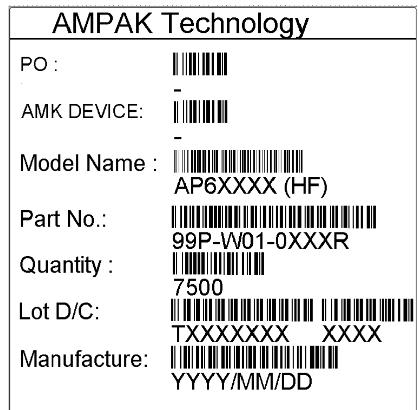
P/N: 99P-W01-0XXXR

Qty : 1500

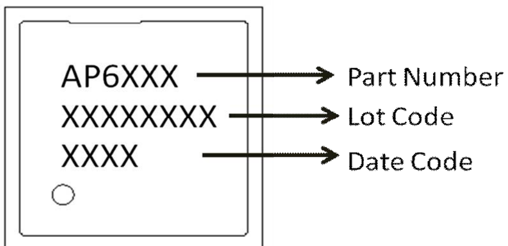
Date Code : XXXX

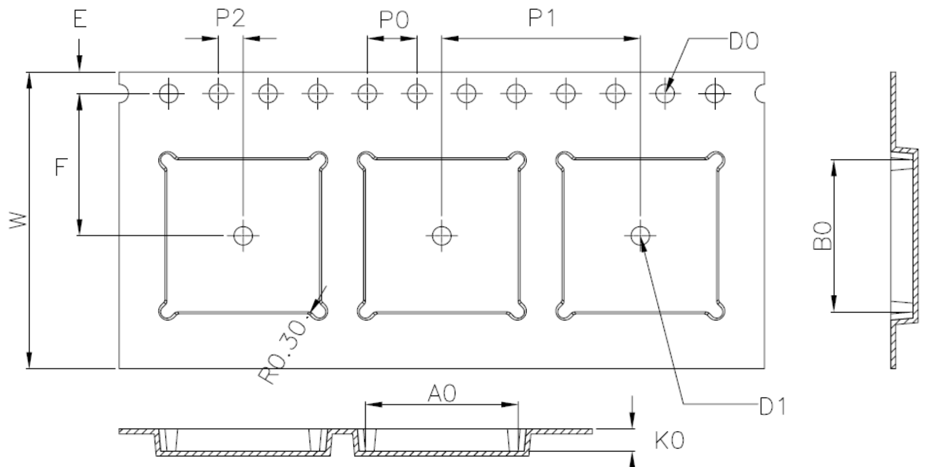
Lot Code : TXXXXXXX

Label D→ Carton box label .



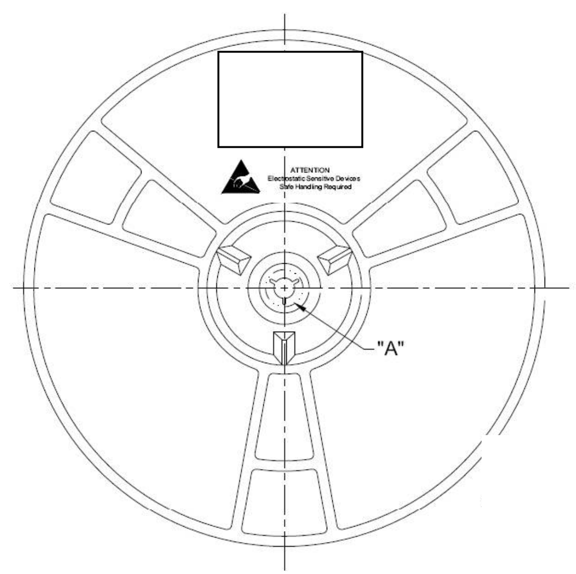
12.2 Dimension

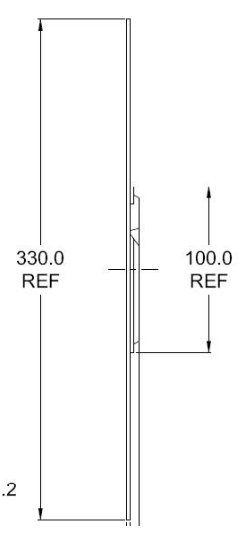




W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	$1.50^{+0.10}_{-0.00}$
D1	Ø1.50MIN

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.





Humidity indicator

Desiccant

B

A

C

C

50mm

338mm

355mm

D

360mm

285mm

375mm

12.3 MSL Level / Storage Condition

Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

1. Calculated shelf life in sealed bag:12months at<40℃and <90% relative humidity(RH)
2. Peak package body temperature: 250 ℃
   If blank,see adjacent bar code label
3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within: 72 hours of factory conditions
   If blank,see adjacent bar code label
   ≤30℃/60% RH,or
   b) Stored per J-STD-033
4. Devices require bake,before mounting,if:
   a) Humidity Indicator Card reads>10% for level 2a-5a devices or>60% for level 2 devices when read at 23±5℃
   b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

Bag Seal Date: ______________________
If blank,see adjacent bar code label

Note:Level and body temperature defined by IPC/JEDEC J-STD-020